Analysis and Modeling of PFC with Appreciable Voltage Ripple to Achieve Fast Transient Response

Ch. Naga Geethika[1], Ch. Sai Babu[2], D. Lenine[3]
[1]PG-Student, Department of Electrical and Electronics Engg.
JNT University, Kakinada, India,
[2]Professor, Department of Electrical and Electronics Engg.
JNT University, Kakinada, India,
[3]Associate Professor, Department of Electrical and Electronics Engg.
RGMCET, Nandyal, India,

ABSTRACT

The classical design of an active power factor corrector (PFC) leads to slow transient response because the compensator used in this circuit is designed with narrow bandwidth. In this paper, the transient response of the PFC can be substantially improved by making the bandwidth of this compensator is relatively wide. It permits certain distortion in the line current that leads to a tradeoff between transient response and harmonic content in the line current. Because of the voltage ripple at the output of the compensator which is considered the control signal, both the static and the dynamic behaviors of the PFC change in comparison with no voltage ripple on the control signal. The static behavior of a PFC with appreciable voltage ripple in the output voltage loop is analysed in this paper by using two parameters: Amplitude of the relative voltage ripple on the control signal and its phase lag angle. These two parameters does not vary with the load and which determine the total harmonic distortion and power factor at the input of the PFC. Finally, the results are verified by MATLAB/ Simulink.

KEYWORDS: *AC-DC boost converter, Modelling, Power supplies.*

I. INTRODUCTION

To limit the harmonic content on the line current of mains-connected equipment, to align the phase angle of incoming current and to limit the total harmonic distortion (THD), the use of an active power factor corrector (PFC) is mandatory. Figure 1 shows a general scheme of an active PFC controlled by two feedback loops. This is the most popular circuitry to control power converters of this type.

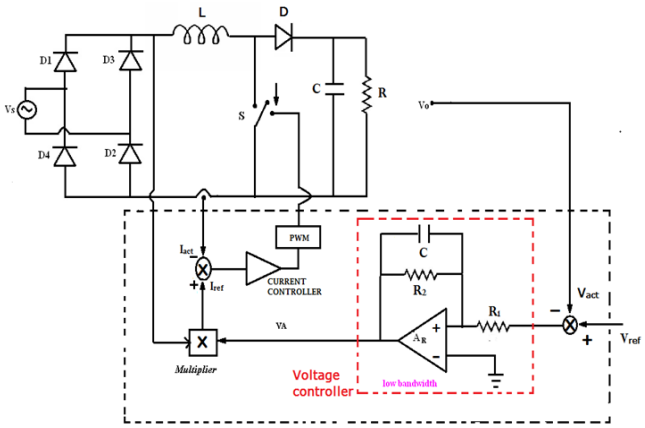


Figure 1. PFC Boost converter with average current mode for Low bandwidth

In this figure, the inner feedback loop is an input-current feedback loop, while the outer one is an output-voltage feedback loop. The current loop makes the line current follow a reference signal, which is obtained by multiplying a rectified sinusoidal waveform (obtained from the line voltage) by the control signal v_A. Thus, the line current i_{gL} is a sinusoid whose amplitude is determined by the value of v_A. The standard design of the voltage feedback loop implies low ripple in v_A. This is because a relatively high ripple would cause considerable distortion in the reference of the line current feedback loop, and hence in the line current.

To have low ripple on the control signal v_A, the bandwidth of the compensator A_R must be relatively low. It leads to a low bandwidth in the entire output-voltage feedback loop. This low bandwidth limits the transient response of the PFC. The transient response of a PFC under these conditions is not fast enough to satisfy the requirements of some loads. However, the transient response of the PFC can be improved by the wide bandwidth.

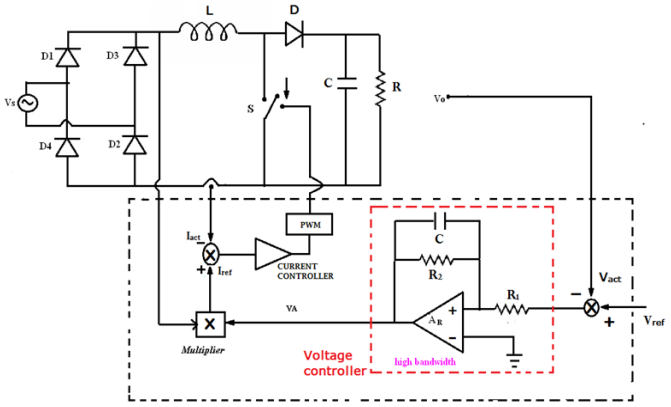


Figure 2. PFC Boost converter with average current mode for Low bandwidth

The transient response is improved for the circuit shown in Figure 2. Because in this circuit, the compensator is designed with high bandwidth. With the voltage ripple at the output of the compensator (which is considered the control signal), both the static and the dynamic behaviors of the PFC change in comparison with no voltage ripple case. Designing of compensator A_R with wide bandwidth results a fast transient response in PFC. It leads to appreciable voltage ripple on the control signal v_A.

The static behavior of PFC with appreciable voltage ripple in the output voltage loop is analysed by using two parameters. Those are the amplitude of the relative voltage ripple on the control signal and its phase lag angle. These two parameters does not vary with the load. But it depends on the total power processed by the PFC converter.

II. MODELING OF OUTPUT VOLTAGE FEEDBACK LOOP

The voltage and the current at the input of the power stage, as shown in Fig: 2, can be written as follows:

$$V_g(\omega_L t) = V_{gp} \,|\sin(\omega_L t)| \qquad (1)$$

$$I_g(\omega_L t) = \frac{V_{gp} \,|\sin(\omega_L t)|\, V_A(t)}{K_M} \qquad (2)$$

Where V_{gp} is the peak value of $V_g(\omega_L t)$

ω_L is the angular frequency of the line

$V_A(t)$ is the output voltage of the compensator

K_M is a constant determined by the controller. The voltage $V_A(t)$ can be rewritten by using the figure below:

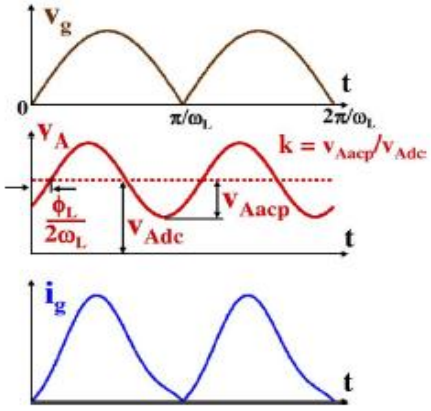


Figure 3. Waveforms in a PFC with appreciable voltage ripple on the control signal V_A

$$V_A(t) = V_{Adc} + V_{Aac}(t) \quad (3)$$

$$V_{Aac}(t) = V_{Aacp}\sin(2\omega_L t - \phi_L) \quad (4)$$

Where V_{Adc} is the dc component of $V_A(t)$

$V_{Aac}(t)$ is the ac component of $V_A(t)$

V_{Aacp} is the amplitude of $V_{Aac}(t)$

ϕ_L is the phase lag angle of $V_{Aac}(t)$

$\frac{\phi_L}{2\omega_L}$ is the delay time between the zero crossing of the line voltage and the zero crossing of the ripple on V_A.

In the PFC circuit, the bulk capacitor C_B filters all the harmonics other than the harmonic of twice the line frequency. Then only a component of twice the line frequency has been considered as the ac component of $V_A(t)$. Moreover, the voltage gain of the compensator A_R at frequencies greater than twice the line frequency will be lower than at twice the line frequency, thus contributing to filtering the harmonics of frequencies higher than twice the line frequency.

III. ESTIMATION OF K AND ϕ_L VALUES

The relative value of the voltage ripple on $V_A(t)$ is defined as follows.

$$K = \frac{V_{Aacp}}{V_{Adc}} \quad (5)$$

This voltage ripple in the output voltage loop is analyzed by using two parameters: its magnitude, V_{Aacp} and its phase lag angle, ϕ_L. As the voltage ripple magnitude can be related to V_{Adc} through k, then V_{Adc}, k and ϕ_L completely define the state of the control variable, $V_A(t)$. Where these values have been expressed as functions of k and ϕ_L and of the power stage variables V_{gp}, V_o and R_L.

In the case of any PFC, this ripple is mainly generated by the current source. The relative output voltage ripple of twice the line frequency is compared with that of four times the line frequency. Only in the case of high values of k (near to 1) and $\varphi_L \approx -90^\circ$ does the value of line frequency become significant.

The steady state expressions can be easily obtained as

$$I_{op} = \frac{2V_0\sqrt{1+k2+2k\sin\phi_L}}{R_L(2+k\sin\phi_L)} \quad (6)$$

$$\phi_L = \cos^{-1}[(V_{Aacp}/V_{Adc})\cos\phi_{R2\omega L}] + \phi_{R2\omega L} - \pi/2 \quad (7)$$

The dc component of the output voltage is related to I_{odc} through the impedance of the R_LC_B cell as:

$$V_{odc} = i_{odc}\,[R_L / (1+R_LC_BS)] \quad (8)$$

IV. SIMULATED RESULTS

The simulation model of the PFC boost converter is maintained at 150V for both low bandwidth and high band width models. The output voltage has been boosted nearly 400V in both cases. From figure 4, the gate pulses given for closed loop PFC boost converter can be observed clearly and the duty cycle of gate signal has been maintained at constant switching frequency (20 KHz).

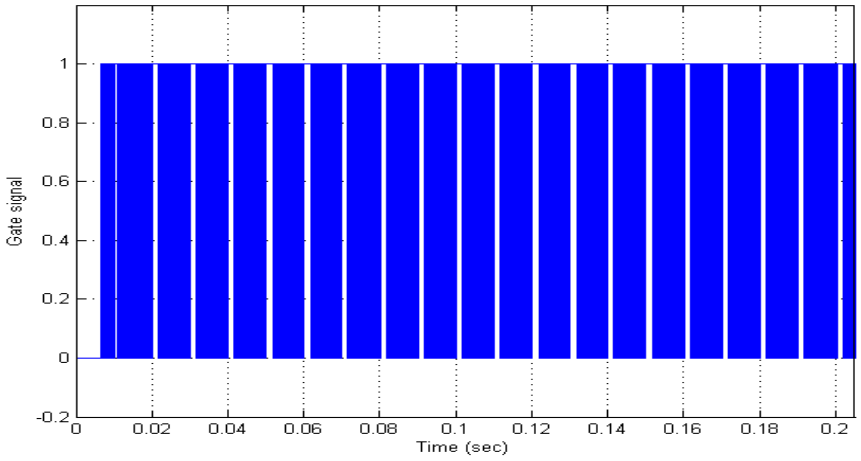
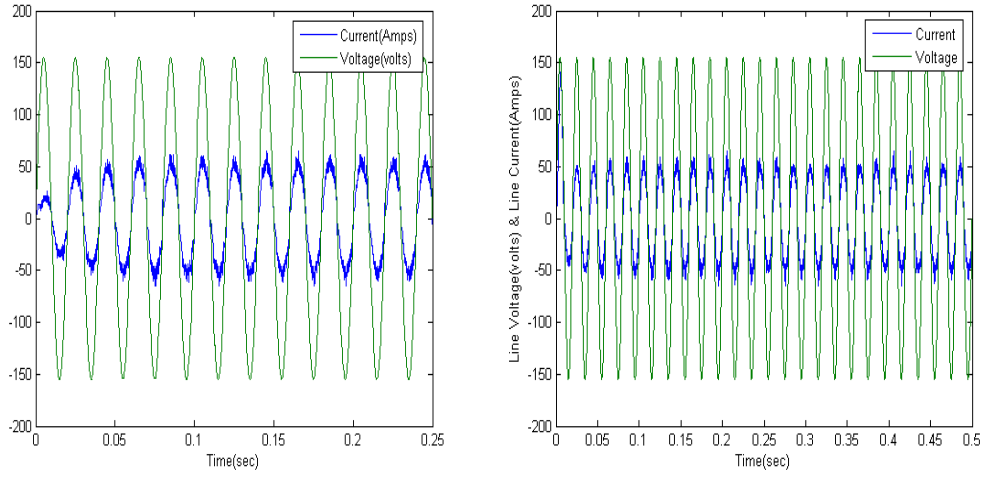


Figure 4. Gate pulses for PFC converter

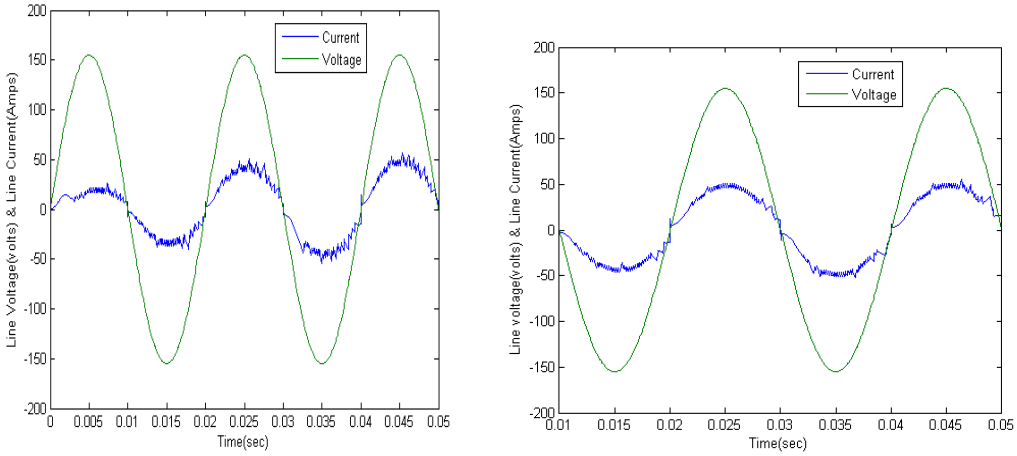
The gate pulses given to the converter are shown in Fig. 4. These pulses are given to IGBT switch in the PFC circuit. The major difference of low bandwidth model from high bandwidth is observed with the variation of the amplitude of the relative voltage ripple (*k*) on the control signal and its phase lag angle (ϕ_L) of the output voltage controller. The input voltage and current to PFC converter for low bandwidth and high bandwidth are shown in Figure 5(a) & 5(b). These two are in phase with each other.



(a) (b)

Figure 5. Input voltage and current response for (a) low bandwidth and (b) high bandwidth models

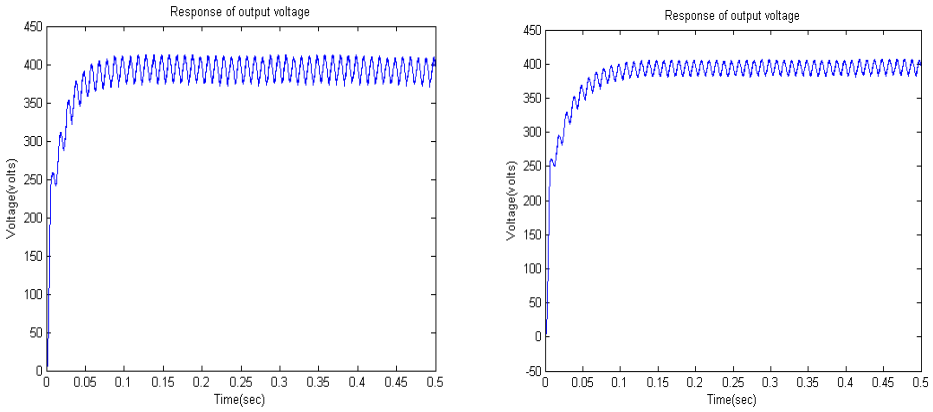
Their steady-state responses are shown in figure 6(a) & (b).



(a) (b)

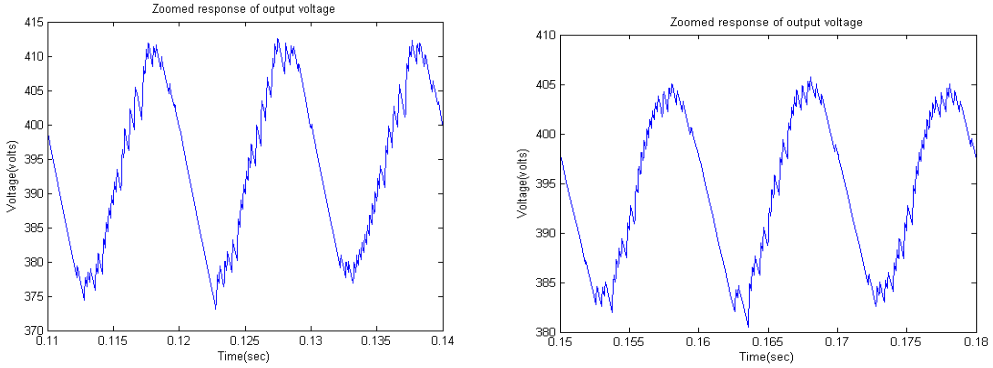
Figure 6: Steady-state response of input voltage and current for (a) low &(b) high bandwidth models

The output response and its steady state response for low and high bandwidth are shown in figure 7 & 8



(a) (b)

Figure 7. Output voltage response of PFC (a) without appreciable voltage ripple (b) with appreciable voltage ripple.

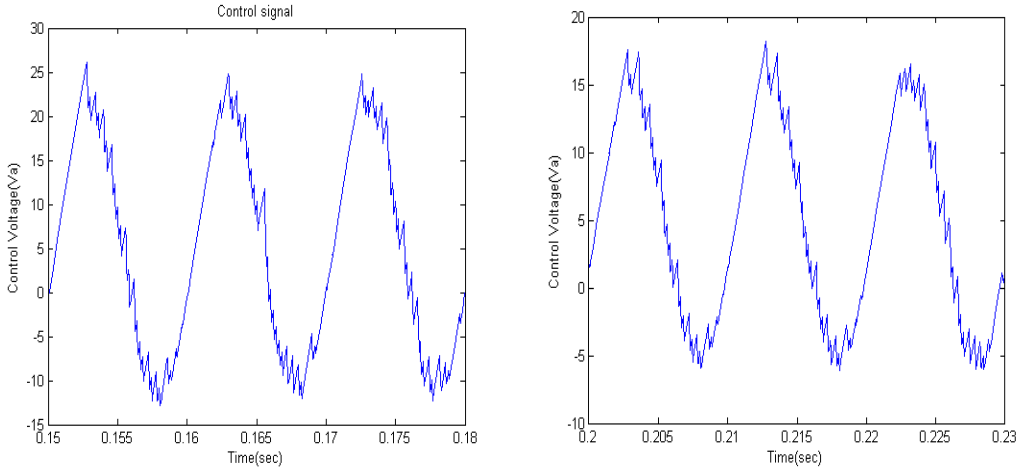


(a) (b)

Figure 8. Steady-state response of output voltage (a) without appreciable voltage ripple (b) with appreciable voltage ripple

From Figure 7& 8, it can be observed that the PF value is high for low bandwidth PFC circuit compared to high bandwidth PFC circuit and distortion is low for low bandwidth. But the transient response is slow for low bandwidth model. For high bandwidth model the transient response is fast and the distortion is considerable.

The control voltage response of low bandwidth and high bandwidth models are shown in figure 9 (a) & (b).



(a) (b)

Figure 9. Control voltage responses of (a) low and (b) high bandwidth models

The Control voltage response of low bandwidth model is shown in Fig: 9 (a). In this Output voltage ripple on the control signal has less magnitude compared to the converter without control technique but is not appreciable value. The Control voltage response of high bandwidth model is shown in Fig: 9 (b). Output voltage ripple on the control signal has less magnitude and it is appreciable value. The static behavior of a PFC with appreciable voltage ripple in the output voltage loop is analysed by using two parameters: Those are the amplitude of the relative voltage ripple on the control signal(k) and its phase lag angle(ϕ_L). All the characteristics of PFC are affected by k and ϕ_L values. Thus, the power processed by the PFC not only depends on the dc value of the control signal, but also on its ripple. High values of the PF and low values of THD are obtained when ϕ_L is positive and the value of *k* is high.

V. CONCLUSION

Power Factor Correction for Average current control technique using PI controller is developed and simulated in MATLAB. Simulation of PFC for low bandwidth and high bandwidth are developed. Output voltage, control signal voltage, gate pulse responses are observed. From the results it is observed that Average current control technique with PI controller gives better power factor correction for different input voltages. The PFC circuit with high bandwidth gives fast transient response. Static behavior of PFC is analysed by using amplitude of the relative voltage ripple on the control signal and its phase lag angle.

REFERENCES

[1] L.Rosetto, G.Spiazzi, P.Tenti "Control Techniques for Power Factor Correction Converters and principle scheme of PFC using boost topology" University of Padova.

[2] Z. Yang and P. C. Sen, "A novel technique to achieve unity power factor and fast transient response in ac-to-dc converters," IEEE Trans. Power Electron., vol. 16, no.6, pp. 764–775, Nov. 2001.

[3] E. Figueres, J. M. Benavent, G. Garcer´a, and M. Pascual, "Robust control of power-factor- correction rectifiers with fast dynamic response," IEEE Trans. Ind. Electron vol. 52, no. 1, pp. 66–76, Feb. 2005.

[4] C. Qiao and K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper," IEEE Trans.Power Electron., vol. 16, no. 3, pp. 360–368, May 2001.

[5] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 814–823, Sep. 1998.

[6] A. Prodic, D. Maksimovic, and R. W. Erickson, "Dead-zone digital controllers for improved dynamic response of low harmonic rectifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 173–181, Jan. 2006.

[7] J. Sebasti´an, M. M. Hernando, A. Fern´andez, P. Villegas, and J. D´ıaz, "Input current shaper based on the series connection of a voltage source and a loss-free resistor," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 583– 591, Mar./Apr. 2001.

[8] J. Sebasti´an,A. Fern´andez, P.Villegas, M. M. Hernando, and J.M. Lopera, "A new active input current shaper for converters with symmetrically driven transformer," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 592–600, Mar./Apr. 2001.

[9] L. Huber, J. Zhang, M. M. Jovanovic, and F. C. Lee, "General topologies of single-stage input-current shaping circuits," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 508–513, Jul. 2001.

[10]P.Mattavelli, G. Spiazzi, and P. Tenti, "Predictive digital control of power factor preregulators with input voltage estimation using disturbance observers," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 140–147, Jan.2005.

[11] A. Prodic, "Compensator design and stability assessment for fast voltage loops of power factor correction rectifiers," *IEEE Trans.* Power *Electron.*,vol. 22, no. 5, pp. 1719–1730,

AUTHORS

Ch.Naga Geethika received the B.Tech(E.E.E) degree from JNTU Kakinada university. Currently she is studying M.Tech in UCEK Kakinada with High Voltage Engineering specialization. Her area of interest is Power systems, Electrical Machines, Power electronics and drives.

Ch. Sai Babu received the B.E from Andhra University (Electrical & Electronics Engineering), M.Tech in Electrical Machines and Industrial Drives from REC, Warangal and Ph.D in Reliability Studies of HVDC Converters from JNTU, Hyderabad. Currently he is working as a Professor in Dept. of EEE in JNTU, Kakinada. He has published several National and International Journals and Conferences. His area of interest is Power Electronics and Drives, Power System Reliability, HVDC Converter Reliability, Optimization of Electrical Systems and Real Time Energy Management.

D. Lenine received the B.Tech (Electrical and Electronics Engineering) degree from Pondicherry University, India and the M.Tech (Electrical Drives and Control) from same University. Currently he is working as Assistant .Profesor in Dept. of EEE, R.G.M. College of Engineering and Technology, Nandyal. He has published/presented nearly six technical research papers in national and international conferences. His field of interest includes Power electronics, Electrical Drives, Digital control of electrical machines and Estimation of machines parameters.