Low Power using Match-Line Sensing in Content Addressable Memory

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ABSTRACT
A Content Addressable Memory (CAM) is hardware search engine in a memory unit that can perform a single clock cycle search operation. Content Addressable Memory is mostly used with the static RAM with the comparison unit to compare data in a single clock cycle leads to more power consumption. This paper proposes a Content Addressable Memory using a NAND cell structure with the comparison unit as parity bit and sensing technique as Match-line Sensing. This architecture reduces the power consumption in Content Addressable Memory based on combination and modification on power saving sensing technique.

KEYWORDS: *NAND, Parity bit, Match-line Sensing, Memory*

I. INTRODUCTION

Content Addressable Memory (CAM) is a hardware storage unit and it is addressed by the data in a parallel data searching circuits. In the standard type of memory, searching of data is addressed by Memory address of an input data. Content Addressable Memory (CAM) is used in applications, where the fast searching of data is required like ATM switches and strong processors. CAM searches an input data in a single clock cycle leads to power hungry during parallel searching. In the conventional CAM, NOR type CAMs cell is used. In this conventional Architecture, power consumption is more because the number of transistors used in the NOR type CAM architecture is more. It's searching speed is high and also the power consumption is also high.

In our design, NOR type CAM cell is modified by the NAND type CAM cell leads to low power consumption with the same speed like a conventional CAM architecture. Number of transistors used in the NAND type cell is less comparing with NOR type cell. CAM has two basic forms: Binary CAM and Ternary CAM. Binary CAM can store and searches the binary data bits zeros (0) and ones (1). Ternary CAM can store and searches the data bits zeros (0), ones (1) and don't care (X). In this proposed modified architecture, by replacing the NOR cell with NAND cell inside the each CAM array leads to power consumption using the match-line sensing technique.

In this paper, Chapter II describes the CAM array design with its searching technique used in the modified CAM architecture. Chapter III describes the performance analysis with its result discussion. The conclusion of the proposed work is given in the Chapter IV.

II. MODIFIED CAM DESIGN

2.1 CAM Cell

Basic CAM celloperatese are often discovered as twofold. One for bit storage in Random Access Memory (RAM) and another for bit comparison i.e. distinctive to CAM as shown in figure 1. At junction transistor i.e. circuit level CAM structure enforced as NAND-type and its variants has been explained by [0000]. However, at branch of knowledge level bit storage uses easy SRAM cell and comparison operate is equivalent to XOR i.e. XNOR logical operation[1]. So our elementary chip cell style is abstracted as a vector product of SRAM and XNOR circuits.

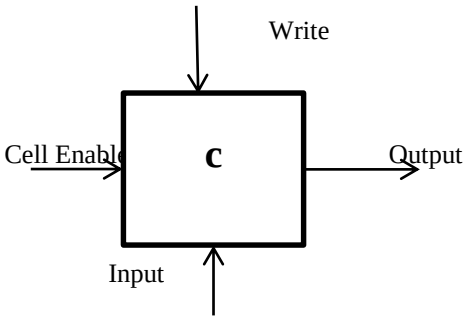

Figure 1 Basic CAM cell

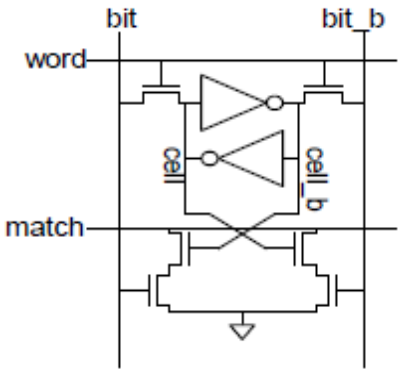

Figure 2 Block Diagram of CAM cell

The basic CAM cell is based on the static memory cell. Data is stored in two cross coupled inverters (SRAM). The word line used to control the two NMOS transistors and permit the CAM to be writing the data [1] as shown in figure 2. The remaining additional transistors are used in CAM for matching the stored and given input data. Static RAM contains two transistors that help to store the bit used for searching. This cell performs browse associated WRITE operations just like an SRAM cell [2]. Next operation is MATCH operation.

2.2 Cam Architecture With Modified Cell

The Modified block diagram of a CAM core contains incorporated search data register and an output encoder. Content Addressable Memory starts comparing operation by loading an n-bit input search word into the search data register. The search data that stored in SRAM are then broadcast into the memory banks through n pairs of complementary search-lines and directly compared with every bit of the stored words using comparison circuits as shown in figure 3.

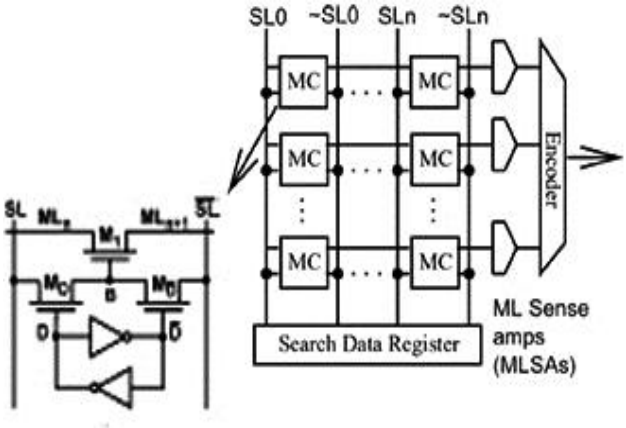

Figure 3 Modified CAM Structure

1. Static RAM Array: There is a wide range of techniques to improve SRAM cell (in fig as MC) performance and power in literature, e.g. dynamic voltage scaling, lower retention voltage etc. But these techniques are not directly related to the CAM operation, and can be applied almost regardless of the chosen CAM cell architecture [3]. Considering SRAM oriented techniques common to all CAM improvement methods in this report, we will not include SRAM optimization in this study, but rather elaborate on CAM specific methods.
2. Match lines (ML): For the conventional CAM design, the ML is precharged, and then evaluated to discharge or stay high based on the match or not match decision of the evaluation circuit [3]. The area, power and delay considerations of the ML routing limits the CAM array size and performance for many applications. In this study we will investigate methods to reduce ML delay, activity factor and power.
3. Search Lines (SL): Conventional CAM design uses complementary search lines, which results in a SL activity factor of 1[2]. This high activity factor shows that SL improvement techniques are crucial for minimizing the CAM power and delay. In this study we present a way to avoid using complementary search lines, and reducing the activity factor to obtain area, power and delay benefits.

2.2.1 NAND cell

The NAND cell helps to implement the comparison between the stored bit D in the array, and corresponding search data on the corresponding searchlines, (SL and$\overline{SL}$),[4] using the three comparison transistors, M_D, $M_{\overline{D}}$and M_1, which are all typically minimum-size to maintain high cell density those stored in the CAM array. The bit-comparison operation of a NAND cell examined by using an example. By considering the case of a match when SL=1 and D=1 and Pass transistor M_D is ON and passes the logic "1" on the search line (SL) to node B where the Node B is the bit-match node which is logic "1" if there is a match in the cell. The logic "1" on node B turns ON transistor M_1.The transistor M_1 is also turned ON in the other match case when SL=0 and D=0 should be noted. During this case, the transistor $M_{\overline{D}}$ passes logic high to raise node B [5] [6]. In other cases in NAND, SL≠D result in a miss-match condition and accordingly node B is logic "0" and the transistor M_1 is OFF. Pass-transistor in node B implementation of the XNOR function. The NAND nature of this cell becomes clear when multiple NAND cells are connected in series. The ML_n and ML_{n+1} node are joined to form a word during this condition [7][8]. A serial nMOS chain of all the M_1 transistors resembles the pull-down path of a CMOS NAND logic gate. The match condition occurs only if every cell in a word is in the match condition for the entire word.

2.3 Match-Line Sensing Technique

Each stored word has a Match-Line (ML) that is shared between the bits to convey the comparison process. Location of the matched word can be identified by an encoder as an output. In the first stage, i.e., pre-charge stage, the MLs is held at the ground voltage level while both SL and $\overline{SL}$ are at V_{dd} [9]. Within the Evaluation stage, complementary search data is broadcast to the SLs and $\overline{SL}$s. Cell transistor and will be turned on, charging up the to a next voltage level, if any mismatch occurs in any CAM. A Match-Line Sense Amplifier (MLSA) is used to detect the voltage change and amplifies it to a full CMOS voltage output. If any does not mismatch happens to cells in a row, no charge up path will be formed and the voltage on the will remain unchanged, indicating a match [10]. Since all available words in the CAMs are compared in parallel, the output should be obtained in a single clock cycle. So, CAMs are faster than other hardware based and software based search applications. They are therefore preferred in high-throughput applications such as network routers and data compressors, where full parallel search operation leads to critical challenges in designing a low-power system for high-speed high-capacity CAMs 1)the power hungry nature due to the high switching activity 2) a huge surge-on current (i.e., Peak current) occurs at the beginning of the search operation due to the concurrent evaluation of the may cause a serious IR drop on the power grid, that affects the operational reliability of the chip[11]. As a result, numerous efforts have been put forth to reduce both the peak and the total dynamic power consumption of the Content Addressable Memory.
A feature of the NAND matchline is that a miss stops signal propagation specified there is no consumption of power past the ultimate matching electronic transistor within the serial nMOS chain. Typically, only one matchline is within the match state [12][13], consequently most matchline have solely a tiny low range of transistors within the chain that area unit ON and so solely a tiny low

quantity of power is consumed. In the new CAM cell incorporates a similar topology of that of the traditional style, their layouts are similar. These two cell layouts have a similar length however completely different heights. Within the new design, V_{DDML} can't be shared between two adjacent rows, leading to a taller cell layout.

III. RESULT AND ANALYSIS

As mentioned in the proposed architecture, data's are stored in the array. Each array store the one bit value. For 4-bit value, four CAM cells are arranged in the series as shown in figure 4, the values are stored in the memory with the address. After the input is given, search line starts charging if anyone of the stored data is matched with given input data is shown in figure 5(X-axis: Time, Y-axis: Voltage).

If the data's not matched, no power should be consumed as shown in figure 6(X-axis: Time, Y-axis: Voltage).. For the matched data and the mismatched data, the power consumption is lesser than the existing NOR architecture.

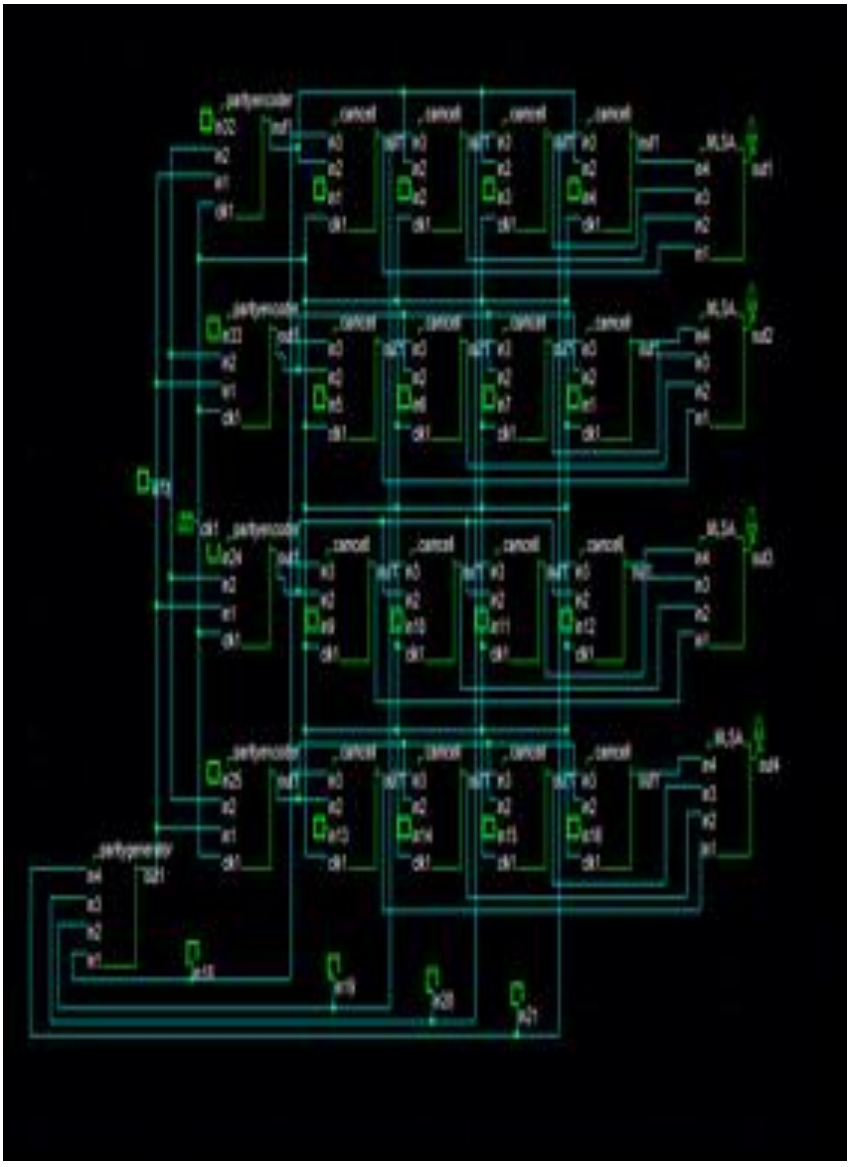

Figure 4 Schematic view of proposed architecture

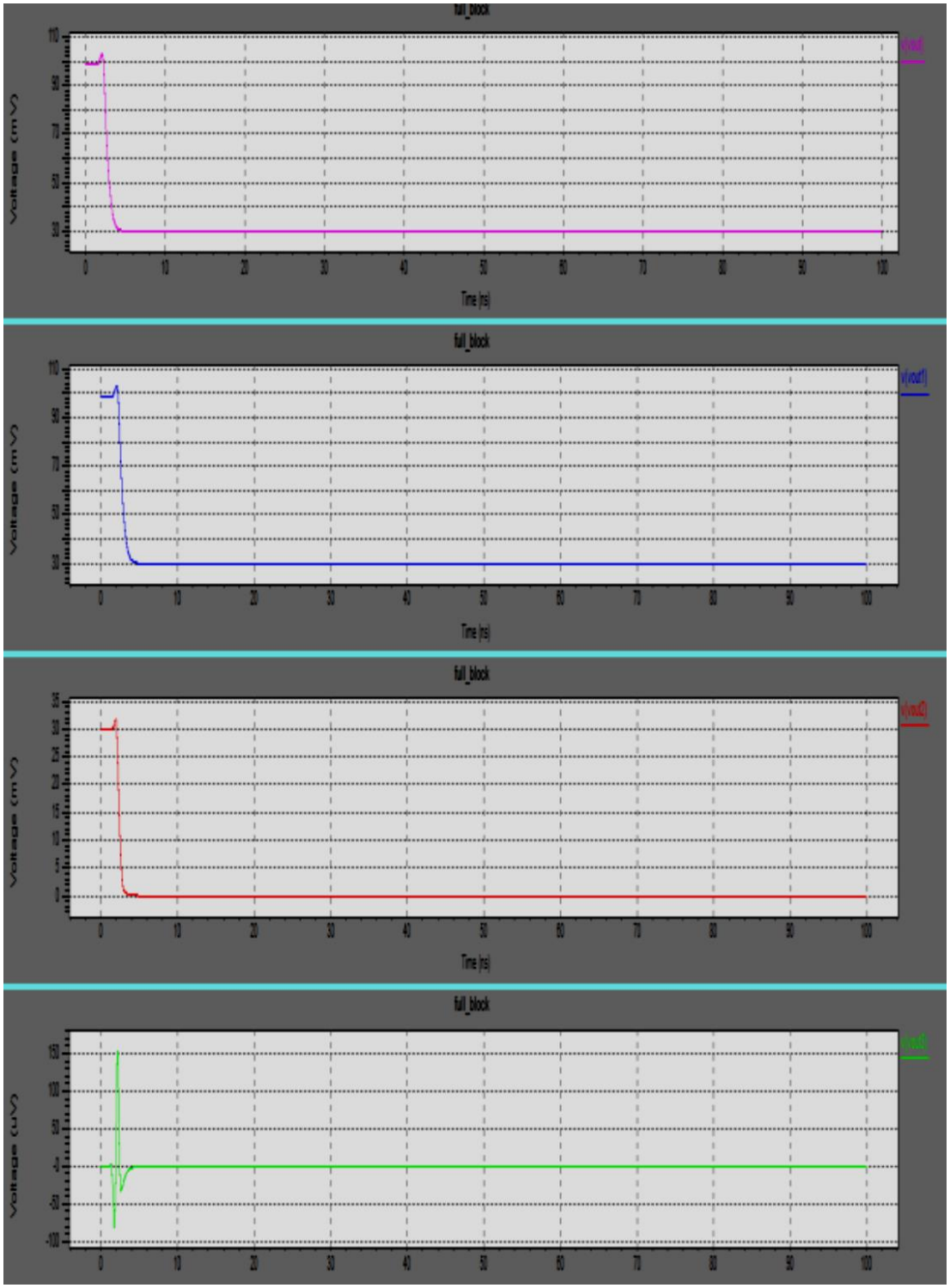

Figure 5 Output waveform for in matched condition

Power analysis for mismatched condition:
Average power consumed → 2.764394e-004 watts
Maximum power →5.882247e-003 at time 6.25e-014
Minimum power →3.156576e-007 at time 9.9923e-008

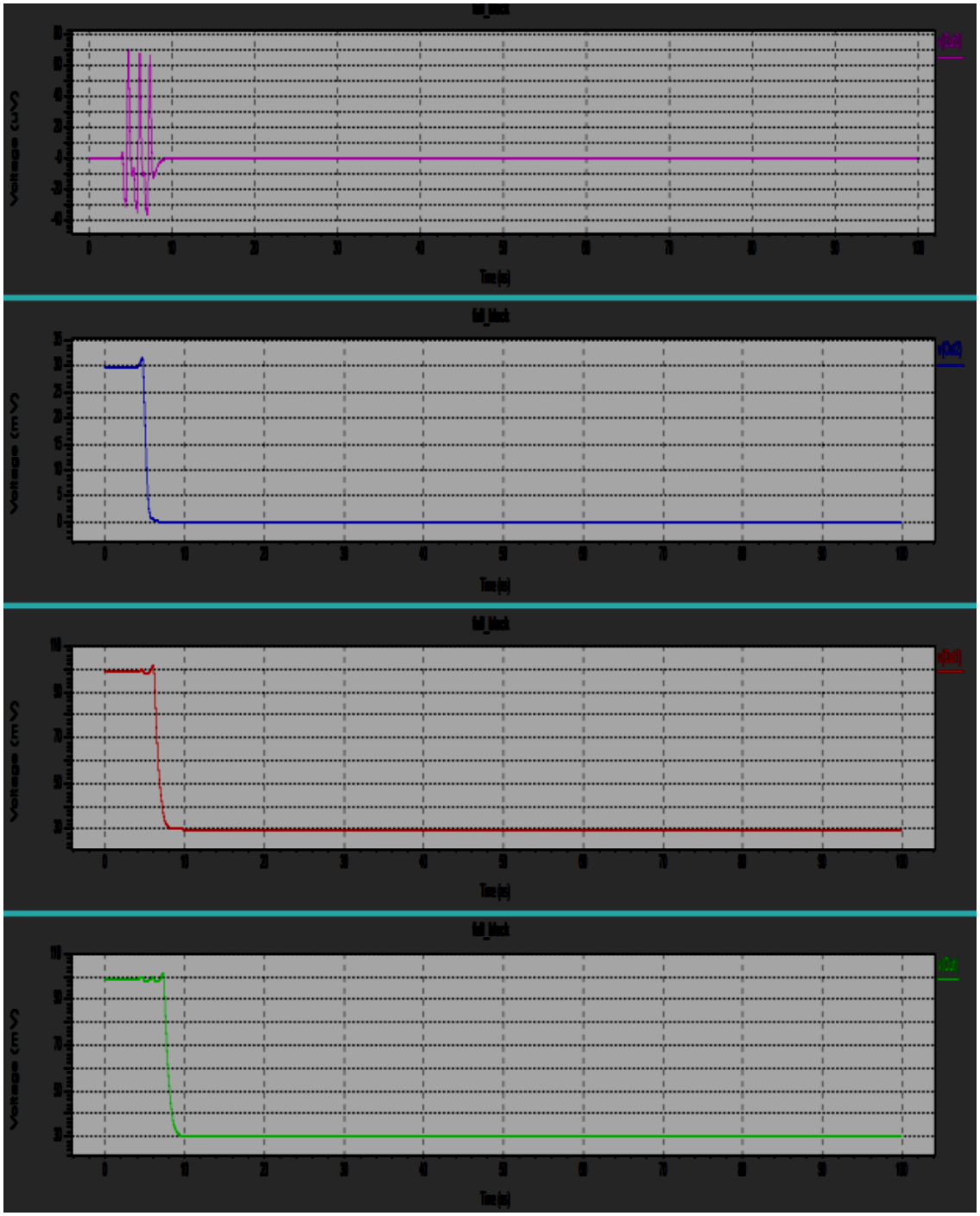

Figure 6 Output waveform in matched condition

Power analysis for matched condition:
Average power consumed → 5.013191e-004 watts
Maximum power →5.112254e-003 at time 6.25e-014
Minimum power →3.756270e-004 at time 9.9993e-008

IV. CONCLUSION

In this theme match-line looking out is dole out by NAND based mostly CAM design. By scrutiny the NAND and NOR, NAND ought to have an occasional power consumption and speed of the NAND CAM conjointly comparatively up to the looking out speed of NOR CAM. By exploitation NAND reduces the whole power consumption within the memory. CAM is ideally fitted to many functions, as well as LAN address search, knowledge compression, pattern-recognition, cache tags, high-

bandwidth address filtering, and quick search of routing, user privilege, security or coding data on a packet-by packet basis for superior knowledge switches, firewalls, bridges and routers. This text discusses many of those applications furthermore as hardware choices for exploitation CAM. CAM may be wont to accelerate any applications starting from local-area networks, management, file-storage management, pattern recognition, computer science, totally associative and processor-specific cache recollections, and cache recollections. Though CAM has several applications, it's notably like-minded to perform any quite search operations.

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