International Journal of Recent Trends in Electrical & Electronics Engg., Apr., 2018.
©IJRTE ISSN: 22316612

A Comprehensive Review on Adiabatic Switching Circuits

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ABSTRACT

The technological evolution has increased the number of transistors for a given die area significantly and increased the switching speed from few MHz to GHz range. This leads to requirements of low power circuits. With the recent developments there have been a lot of technological evolutions one such evolution is adiabatic switching circuits. It should be noted that for adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat.

KEYWORDS: *Adiabatic, Reversible Logic, ASIP, ASIC, Instruction set*

I. INTRODUCTION

Designing electronic systems using digital techniques has become a well-accepted standard with electronic design community. The precision and speed of any computational block in digital design can be increased by just widening the data bus and making computational blocks compatible with widened data bus [1]. Thus a complex digital electronic system handles wide data buses, addresses large memory space and embeds the logical and computational blocks with appropriate data bits to match the widened data bus [2,3,4]. Due to the typical features of CMOS technology, for integrating complex systems in small silicon area with fairly low power dissipation at speeds demanded by most of the applications, CMOS VLSI has been the obvious choice of designers [5,6]. About 90% of the total electronic systems use CMOS technology at the back end. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed. In present work attempts are made to review adiabatic logic circuits. The present work focuses on carefully studying adiabatic developments [7, 8]. The study and survey of the different types of adiabatic logic circuits is carried out. The study survey and comparison of the different types of CMOS based logic circuits with adiabatic logic circuits is also done. In literature, there are two kinds of adiabatic circuits presented one is full-adiabatic and other is quasi-adiabatic or partial adiabatic circuits [9, 10]. Rest of the paper is organized as follows the section to covers related work whereas section finally section 3 covers conclusion and future research directions.

II. RELATED WORK

Paul Leroux, et.al. gave Design and Assessment of a Circuit and Layout Level Radiation Hardened CMOS VCSEL Driver. They gave the radiation laborious style of a 155 Mb/s, 0.7 m CMOS driver for a vertical-cavity surface-emitting laser (VCSEL). The circuit options increased tolerance to radiation evoked shifts within the device characteristics by using a replica-based feedback mechanism. The layout was achieved

with the help of an in-house developed radiation hardened part library. At an occasional rate of 4.5 Gy/h or 450 rad/h, the output current remains constant up to a minimum of 3.5 kGy. At a rate of 21 kGy/h, the output current of the motive force drops by 100% at a dose of 3.5 MGy and breaks down utterly at 5.5 MGy [12].

Diego Mateo and Antonio Rubio in 1998 proposed a design and Implementation of a Multiplier in a Quasi-Adiabatic Ternary CMOS Logic. Adiabatic switch could be a technique to style low power digital IC's. Totally adiabatic logics have costly silicon space necessities. To resolve this disadvantage, a quasi-adiabatic ternary logic is projected. Its basis is conferred, Results show a satisfactory power saving with regard to standard and alternative quasi-adiabatic binary multipliers, and a decrease of the area required with regard to a completely adiabatic binary one [13].

Joohee Kim Conrad et.al. In 2002 suggested an Energy Recovering Static Memory suggested an energy-recovering adiabatic static RAM with a unique driver that moderates power dissipation by effectively recovering energy from the bit/word line capacitors. Energized by a single-phase ac power-clock, the proposed SRAM delivers browse and write operations with single-cycle latency. Thereto finish, a precharge-low scheme is employed along with a modified sense amplifier design that achieves high efficiency at differential voltages. Feedback circuitry from the driver output to the control circuit ensures that our driver remains efficient, not dependent on of the access pattern. The energy convalescent SRAM functions properly whereas achieving substantial energy savings over a large spread of clock voltages and operative frequencies. H zest recreations of a direct full custom adiabatic 256x256 SRAM, that has the vitality recouping bit/word line drivers, the cell cluster, and the sense amplifiers, appear more than 2.6x vitality reserve funds at 3V, 300MHz as contrasted and its standard partner [14]. Energy Transfer and Recovery Efficiencies for Adiabatic Charging with Various Driving Waveforms was given by Michael P. Frank and Marco Ottavi in 2006. A standard drawback that arises within the study of energy-recovering circuits for digital logic is to investigate the relative energy potency of various attainable voltage waveforms for the power/clock signals that are accustomed drive adiabatic charge transfers within the logic. To well characterize these wave form potency problems provides an analytical tool that's useful within the style improvement of economical power/clock signal generators. during this note, acceptable metrics for the comparison of the energy efficiencies of various voltage waveforms within the context of necessities on the energy transferred to the logic load or the energy provided by the power/clock resonator, and show however these potency metrics scale as functions of frequency for a variety of easy wave shapes during a basic lumped-element circuit model [15].

Prasad D Khandekar, et al. in year 2010 suggested Implementation and Analysis of Quasi-Adiabatic Inverters. They mentioned the implementation of 3 quasi-adiabatic logic designs and analyzes the charge flow. All the NOT gate circuits are styled with the help of 180nm technology in Cadence design setting [16].

Ke Wu, et.al. Designed a Low-Voltage True-Single-Phase-Clocking (TSPC) Logic using Bulk Dynamic Threshold MOS Technique. Their work concerned a replacement quick Bulk True Single phase duration (TSPC) based scheme. Dynamic Threshold MOS technique for each NMOS and PMOS was introduced. In planned methodology the common substrate of the NMOS logic or PMOS logic was dynamically controlled: the potential changes if only these transistors ought to work and keeps high threshold after they are stop working. And also the theme uses the charge recovery technique of the substrate to more scale back power. It's capable of in operation at 0.8V or maybe lower. The planned theme is shown to be 33.45% quicker and has 20.86% energy savings compared to the regular TSPC logic circuits, throughout HSPICE simulation [17].

Prasad D Khandekar, and Dr. Mrs. Shaila Subbaraman gave a novel architecture for Low Power 2:1 MUX for Barrel Shifter. Barrel Shifter is a very important block within the processor design and not a lot of effort has been done to reduce its power dissipation. A barrel shifter wants n MUX for n-bit shifting and thus planning a MUX for low power to use it as a repetitive block within the barrel shifter can significantly cut back the simulation time. The end result of the analysis provided pointers for planning barrel shifter with the help of immoderate low power MUX [18].

Prasad D Khandekar and Shaila Subbaraman suggested in another paper a Low Power Inverter and Barrel Shifter Design using adiabatic principle, since most of the scientific applications need floating point computations that need barrel shifter as the major element for hardware implementation and since not a lot of efforts are according to be taken by the researchers to attenuate its power dissipation, it's planned to implement barrel shifter with the help of adiabatic logic. A barrel shifter wants n log n multiplexers for n-bit shifting. Therefore planning a low power MUX for employing as a repetitive block within the barrel shifter can significantly cut back the power dissipation in barrel shifter. The simulation results compared the power and delay parameters of basic multiplexer with the help of typical CMOS approach and adiabatic logic approach [19].

Tadahiro Kuroda and Mototsugu Hamada proposed Low-Power CMOS Digital Design with Dual Embedded Adaptive Power Supplies. In their work they given a low-power CMOS style methodology with twin embedded adaptive power supplies. It's found that the lower supply voltage ought to be set at 0.7 of the upper supply voltage to attenuate chip power dissipation. This information aids researchers in deciding the optimum supply voltages inside a restricted design time. An MEPG-4 video codec chip is intended at 2.5 and 1.75 V for internal circuits that are generated from an external power supply of 3.3 V by the dual-VS circuits. Power dissipation is reduced by 57 while not degrading circuit performance compared to a traditional CMOS style [20].

Low-Power, Low-Noise Adder Design with Pass-transistor Adiabatic Logic was proposed by Hamid Mahmoodi-Meimand and Ali Afzali-Kusha. The potency of a completely adiabatic logic circuit is compared with its combinative and pipelined static CMOS counterparts. An 8-bit carry look-ahead adder id developed employing a 0.6-pm CMOS technology for all 3 logic designs. Supported on the post-layout simulation results, the adiabatic adder exhibits energy savings of 76% to eighty seven % and eighty seven% to 90% compared to its combinative and pipelined static CMOS counterparts, severally. It conjointly exhibits a substantial reduction in switching noise, compared to its static CMOS counterparts [21].

Joonho Lim, etal proposed NMOS Reversible Energy Recovery Logic for Ultra-Low-Energy Applications. It is a completely reversible adiabatic logic, NMOS reversible energy recovery logic (NRERL), that uses NMOS transistors solely and an easier 6-phase clocked power. Authors expressed that at low-speed operation, space overhead and energy consumption are smaller, compared with the other totally adiabatic logics. Bootstrapped NMOS switches are utilized to alter the NRERL circuits [22].

Balaji Narasimham, etal developed a new on-chip single-event transient (SET) check structure to autonomously characterize the widths of random SET pulses. Simulation results showed that the measure coarseness rapidly scales down with technology. Conjointly the experimental results indicated pulse widths variable from regarding 900 psec to over3 nsec because the laser energy was enhanced [23].

Samik Samanta gave in his work a Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSI-EDA Tool, he applied adiabatic logic style approach to style COMS NOT Gate. Author designed and simulated PFAL NOT gates and power dissipation is compared with the static CMOS inverter [24].

Massimo Alioto and Gaetano Palumbo recommended Power Estimation in adiabatic Circuits: a simple and accurate Model, they planned a technique supported by a linearization of the circuit and simplifying the analytical result obtained on the equivalent network. The approach ends up in easy relationships which may be used for a pencil-and-paper analysis or enforced on computer code. The accuracy of the results is validated by means that of Spice simulations on an adiabatic full adder designed with a 0.8m technology [25].

Shun Li et.al presented a new technique Quasi-Static Energy Recovery Logic with Single Power-Clock Supply. Authors presented a new Quasi-Static Single part Energy Recovery Logic (QSSERL) that, not like the other existing adiabatic logic family, uses single ac supply-clock without extra voltages. This not solely ensures lower energy dissipation, however conjointly simplifies the clock style which might be otherwise additional difficult as a result of the signal synchronization demand. It's demonstrated that QSSERL circuits operated as quick as typical two-phase energy recovery logic counterparts. HSPICE simulation with an 8-bit logarithmic Look ahead Adder (LLA) employing static CMOS,CAL (an existing single-phase primarily

based energy recovery logic), and QSSERL showed that the QSSERL adder consumes solely fifty six of energy like its static CMOS counterpart at 10MHz and achieves higher energy potency than CAL [82].
Xu Jian etal suggested a Research of Adiabatic Multiplier Based on CTGAL. They planned a brand new adiabatic multiplexer supported by the investigation of Clocked Transmission Gate adiabatic Logic (CTGAL) circuit, in their paper. It comprises of a halfway item generator, a fractional item compressor and a parallel prefix snake. CTGAL is employed altogether the circuits to charge and discharge the node capacitances while not the threshold value losing and therefore the charge on the output node capacitances are often recovered fully. Therefore the power consumption of the freshly designed circuits is considerably reduced [26].
M. Hempstead proposed an application specific design that integrates an event processor that assists main microcontroller executing needed system tasks. The given approach guarantees smart power improvement; however, no real world implementation results are given [27]. The approach in [28] utilizes hardware acceleration and optimized radio in a highly integrated single-chip solution. It applies an 8- bit data, 16-bit instruction CPU with reported size of 0.381 mm2 in a 0.25um process. The reduction of power in sensing element node radio is additionally investigated. One novel approach to low power radio is given in Pico Radio project [29]. Some researchers propose use of wake-up radio so as to scale back the radio power. Wakeup radio serves as a low-power switch to the node transceiver [30]. The implementation of advanced power-saving techniques such as dynamic voltage scaling [31] and power gating [32] promises to deliver additional reduction of node power consumption. The energy harvest is additionally thought-about as a possible resolution to increase the battery life [33]. Employing an asynchronous processor within the style of a detector node is planned in [34]. Another solution is an asynchronous architecture of a sensor node presented in [35]. The later solution includes additionally an energy harvesting circuit. However, no implementation results for those solutions have been presented. Fully asynchronous design is troublesome to implement and it needs all peripherals to own committed asynchronous interface.
The idea of instruction set bound ASIPs is accepted within the technical literature. During a crisp summary of ASIP style problems [36] is given. The reviewed ASIP style flows are targeted at performance constraints and don't take under consideration the energy consumption of the implementation. Moreover, the represented style flows often separate ASIP architectural style space exploration from ASIP instruction set synthesis. Within the current work, these style steps are combined, as a result of the instruction set is viewed as an interface to the design with mutual dependencies. As a consequence, design and instruction set are conjointly optimized so as to get optimum results. There are numerous ASIP style tools for the whole ASIP style flow from application to implementation. In the PEAS [37] style surroundings is represented that creates a direction set reenactment display and a synthesizable model from a design processor portrayal. The MetaCore DSP development system [38] is an ASIP style tool that supports style space exploration and design generation. Within the style flow, the development tools like compiler, assembler, and ISA machine likewise because the HDL description of the processor are generated. In [39] the ISDL machine description language is employed to come up with a little true instruction level machine and a synthesizable Verilog processor description. There are some style tools given within the literature that specialize in a set of the ASIP style flow. A framework for Compiler-ASIP co-design with feedback from an optimizing compiler to the ASIP style is represented in [40]. In [41] the RECORD compiler is given that uses a structural RTL model of a DSP as a start line of the compiler generation. In [42] authors proposed an extremely economical processor style methodology supported by the LISA 2.0 language. Generally the design style section is dominated by a repetitive processor model refinement based on the results of hardware and code simulation and identification.

III. CONCLUSION & FUTURE WORK

Adiabatic Switching circuits are finding widespread use in day to day life. The efficiency, lifetime& reliability of the circuit depend upon power consumption. If an adiabatic switching circuit is designed it will not only decrease the power requirement, but also conserve the circuit energy rather than dissipating it as heat.

a. By designing SRAM based on Adiabatic Switching circuits designers will be able to achieve following:

- Power dissipation is the main constrain when it comes to Portability. The mobile device consumer demands more features and extended battery life at a lower cost.
- About 70% of users demand longer talk and stand-by time as primary mobile phone feature. Top 3G requirement for operators is power efficiency.
- Customers want smaller & sleeker mobile devices. This requires high levels of Silicon integration in advanced processes, but advanced processes have low power efficiency which can be optimized by SRAM based on Adiabatic Switching circuits.
- The growing market of portable (e.g., cellular phones, gaming consoles, etc.), battery-powered electronic systems demands SRAM design with ultra-low power dissipation.
- As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of SRAM based on Adiabatic Switching circuits.

b. Effective SRAM based on Adiabatic Switching circuits increases optimization at all design abstraction layers as:

- **System:** Partitioning, Power down
- **Algorithm:** Complexity, Concurrency, Regularity
- **Architecture:** Parallelism, Pipelining, Redundancy, Data Encoding
- **Circuit Logic:** Logic Styles, Energy Recovery, Transistor Sizing
- **Technology:** Threshold Reduction, Multi-threshold Devices.

c. Helps firms monetize their innovations and grow by improving:

- Packaging and Cooling costs.
- Digital noise immunity.
- Battery life (in portable systems)

d. Helps small and medium enterprises (SMEs)

- Custom designed SRAM based on Adiabatic Switching circuits will help small and medium enterprises, design cost effective, highly reliable and environment friendly devices requiring energy efficient storage elements.

e. Benefits consumers and society

- SRAM based on Adiabatic Switching circuits provide consumers with innovative products and services in virtually every area of life, and helps protect consumers from low performance power hungry products.
- Improved battery life hence better performance, value for money, reliability etc.
- Environmental concerns.

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