Adiabatic SRAM for Low Power Devices

Amit Saxena[1], Kshitij Shinghal[2], Deepti Shinghal[1]

[1]Assistant Professor, [2]Associate Professor,
Deptt. of E& C Engg, Moradabad Institute of Technology, Moradabad, India
[1]Research Scholar, Monad University, Hapur, India

ABSTRACT

With modernization and requirement of computational devices having facility of having communication anytime anywhere, there is an ever-increasing demand of battery operated handheld portable devices which are small in size, low cost, reliable and consumes low power. Analysis has proved that memory array consumes more 60 % power and poses maximum power constraints on hand held and portable devices. This power constraint has led to the requirement of Low power memories for such devices. The power consumption of SRAM varies widely depending on how frequently it is accessed and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower frequency, such as in applications with moderately clocked microprocessors, draws very little power and can have a nearly negligible power consumption when sitting idle – in the region of a few micro-watts. Several techniques have been proposed to manage power consumption of SRAM-based memory structures. In this paper a robust adiabatic SRAM is designed. The main aim is to use adiabatic switching circuits to compensate throughput degradation, so a medium throughput for SRAM can be achieved. Proposed architecture is designed using adiabatic switching principles. Proposed adiabatic SRAM is tested using OrCAD PSPICE. The results show that performance of adiabatic SRAM is better than other contemporary SRAMs

KEYWORDS: Adiabatic, Reversible Logic, Memories, SRAM, Low power memories, Static Memory, dynamic power, static power.

I.   INTRODUCTION

Over the past few decades, power reduction techniques in memory circuits have progressively geared up the list of researcher's design concerns, over the rising cost of energy, and an increasing sensitivity to green practices, low power consumption and the like, have become a major concern for design engineers. In order to reduce the power consumption in case of memories, different classical approaches were adapted and proposed by the design engineers. Since due to the attractiveness of major battery operated electronic devices and handheld mobile devices, the power consumption in SRAM cell is pointed out as one of the major concern in the high-performance chips. Also the SRAM consumes large fraction of total power and die area in high performance embedded processors therefore the designing low-power adiabatic SRAM is somewhat more complicated. The more power will be consumed in the standby mode due to the result of enhanced leakage current of the memory. Many of the schemes have proposed & reported the improvement in the power consumption in memory devices, by reducing the leakage current. In, a completely unique adiabatic SRAM bit cell appropriate for subthreshold operation was projected and achieved vital reduction in leakage current and roughly 50 percent reduction in read/write power compared to the standard 6T cell. In present work attempts are made to design an adiabatic SRAM for low power computational devices. The present work focuses on limiting the power dissipation at System level. Rest of the paper is organized as follows the section to covers literature review whereas section 3 gives Structure of Proposed adiabatic SRAM in section 4 Design of the

adiabatic SRAM is covered finally section 5 covers results and discussions at the end paper is completed with conclusion and future research directions.

II. LITERATURE REVIEW

S. Kanchana Bhaaskaran et. al. presented the design and performance analysis of the dual-rail encoded and sense amplifier structured 2N_2P, 2N_2N2P, IPGL and PFAL quasi-adiabatic circuits operated by two-phase sinusoidal power-clock sources. The energetics of those families are studied for variable power-clock voltages. The drivability characteristics were evaluated with the help of capacitive loads. The performance validation is formed through 8-bit & 16-bit adder circuits employing an integrated power-clock generator. Best adiabatic gain values are achieved for 2N_2N2P and IPGL circuits across a large frequency vary. Energy recovery comparison between the four part ramp and two-phase trigonometric function power-clocks is formed. The results demonstrate the potency of curved power clock at each the high and also the low frequency ranges of operation. The circuits were designed using 180 nm CMOS technology [1]. Prasad D Khandekar et. al. highlighted within their work sharply increasing demands for moveable electronic devices has strengthened the necessity of low power style methodologies in the recent years. Adiabatic logic vogue is evidenced to be a gorgeous resolution for low power digital style. The energy is recycled back to power provide rather than being wasted. Several researchers have introduced completely different adiabatic logic designs within the past few years. This paper discusses the implementation of 3 quasi-adiabatic logic designs and analyzes the charge flow. All the electrical converter circuits are styled employing 180nm technology in Cadence design surroundings. [2]. Nakata, Shunji et. al. 2010 designed an adiabatic 64-kb SRAM circuit with shared reading and writing ports that permits gradual charging and discharging whereas maintaining an oversized VDD in order that the issues of VT variation and electro-migration within the nanocircuit are often resolved. Within the writing mode, the voltage of the memory cell ground line is enhanced to VDD/2 step by step, and therefore the nMOSFET is turned off in order that the memory cell ground line is ready in an exceedingly high-impedance state. Information will then be written simply by decreasing the voltage of 1 bit line adiabatically, whereas the voltage of the opposite bit line remains high. For reading, with the help of the shared reading port, the voltage swing of the world bit-line are often weakened to VDD/4 in order that the issues of electro-migration are often resolved. The reading methodology permits a gradual current flow within the memory cell. They designed the cell layout and confirmed that the amount of transistors within the cell is quasi-six. Additionally, 2 forms of new step voltage circuits with tank capacitors are planned. One is for designing the memory cell ground line voltage and therefore the remaining for charging the word line voltage adiabatically. Spontaneous step voltage formation is confirmed experimentally [3]. Hong Li, Linfeng Li, and Jianping Hu in 2010 showed that with rapid technology scaling, the proportion of the static power consumption catches up with dynamic power consumption bit by bit. To decrease leak consumption is turning into a lot of vital in low-power style. In this paper, a power-gating theme for P-DTGAL (p-type dual transmission gate adiabatic logic) circuits to cut back outflow power dissipations below deep submicron method is proposed. The energy dissipations of P-DTGAL circuits with power-gating theme are investigated in several processes, frequencies and active ratios. BSIM4 model is adopted to mirror the characteristics of the outflow currents. HSPICE simulations suggested that the leakage loss is greatly reduced by using the P-DTGAL with power-gating techniques [4]. Yadav, R.K. et. al. in 2011 gave that the Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network is decreased and a few of energy hold on at load capacitance is recycled rather than dissipated as heat. However the adiabatic technique is extremely smitten by parameter variation. With the assistance of TSPICE simulations, the energy consumption is analyzed by variation of parameter. In analysis, 2 logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback adiabatic Logic) are compared with typical CMOS logic for inverters and 2:1 mux circuits. It was observed that adiabatic technique can be used alternatively for low power application in nominative frequency vary [5]. Yadav et. al. proposed that the energy consumption issue is efficiently addressed by adiabatic switching technique in design of low power digital circuits. Adiabatic shifting technique offers the reducing in energy dissipletion throughout shifting events and employing the load capacitance energy rather than dissipating it as heat. However adiabatic circuits extremely rely on power clock and parameter variations. With the assistance of clocking rule, the digital

circuits like NOT & NOT chain are designed for adiabatic techniques, 2N-2N2P, economical Charge Recovery Logic (ECRL), feedback adiabatic Logic (PFAL) and Clocked adiabatic Logic (CAL) exploitation TSPICE simulation. The results suggested high energy savings as compared to CMOS circuits in specified frequency range [6]. Patpatia et. al. presented new design techniques for adiabatic full adder cell. Adiabatic logic is that the best energy saving technique that provides terribly low power dissipation in integrated circuits. Adiabatic Full adder is simulated by employing totally different adiabatic techniques. Simulation results advised that energy loss of adiabatic circuits will be greatly reduced if Complementary Pass semiconductor adiabatic Logic technique is preferred. All the circuits have been simulated on BSIM3V3 90nm technology on tanner EDA tool [7].

Mihail Cutitaru et. al. found that power dissipation reduction is that the core principle in creating any electronic product moveable. Although there has been a decrease in circuit in operation voltages, vital power is lost in change components (transistors). This has given rise to a replacement means of computing – adiabatic computing, wherever vital energy savings are achieved by employing time-varying clocks. This paper provides an evidence of however adiabatic computing works and conferred many adiabatic families and their blessings and downsides. A replacement single-phase adiabatic family buffer/inverter that uses sixty eight less energy than its CMOS equivalent was planned [8]. Mukesh Tiwari et. al. presented that electronic systems have challenged the research project towards the study of technological, architectural and circuital solutions that permit a discount of the energy dissipated by an electronic circuit. Such a part of the overall power dissipated by a circuit is named dynamic power. So as to scale back the dynamic power, an alternate approach to the standard techniques of power consumption reduction, named adiabatic shift technique is use. Adiabatic shift is an approach to low-power digital circuits that differs essentially from alternative sensible low-power techniques. The term adiabatic comes from physical science, wont to describe a method during which there's no exchange of warmth with the surroundings. Once adiabatic shift is employed, the signal energies keep on circuit capacitances could also be recycled rather than dissipated as heat. The adiabatic shift technique can do terribly low power dissipation, however at the expense of circuit complexness. Adiabatic logic offers method to employ the energy keep within the load capacitors instead of the standard way of discharging the load capacitors to the bottom and wasting this energy. Power reduction is achieved by convalescent the energy within the recover part of the supply clock [9]. Sunil Kumar Ojha presented a new static random access memory (SRAM) cell. The projected SRAM cell used 2 trapezoidal-wave pulses and resembles behavior of static CMOS 4T-SRAM. The elementary cell structure of projected SRAM cell consists of 2 high load resistors that are made of PMOS, and NMOS switch that is important to limit short current. From the simulation results, work suggested that the energy consumption of the proposed circuit is lower than that of conventional SRAM cell [10].

Swathi Tangella and Prema Kumar Medapati reviewed that fast advances within the field of VLSI system styles brought memory circuits are endlessly regulated and successively, additional variety of cells may have created potential to integrate on tiny chip. But in Nano scale SRAM there's giant variation of threshold voltage happens. To resolve threshold voltage variation downside in SRAM in their work they projected the adiabatic SRAM cell and later they introduced a NBTI SRAM that effectively reduces the matter. This paper was carried out by using Tanner EDA Tools [11]. Munukuntla Chandra Shekar Reddy et.al. in et.al. 2015 said that SRAM, being a key component of the processing system of sensor nodes, has to satisfy the low-power requirement as well. As feature size shrinks, the key part of power consumption are going to be discharge. Within the past five years, there has been important effort to seek out ways in which to scale back discharge, amongst them area unit offer voltage scaling, idle mode implementation and body biasing. Whereas the prevailing solutions offer smart discharge reduction, they largely target microchip cache, with circuit performance being a vital parameter to be optimized. The ability discharge is reduced, by coming up with the SRAM circuit with single bitline. To scale back the discharge from this circuit whereas exercise the Negative Bias Temperature Instability based mostly SRAM circuit is enforced. This reduces the discharge from the SRAM circuit and additionally will increase the browse stability within the circuit. Coming up with and verification of the circuit is completed in TANNER EDA [12]. In their work, Yuejie Zhang, Jianping Hu, Tianfang Ma, Beibei Qi in 2015 proposed a FinFET SRAM is verified by employing adiabatic computing. All the circuits of the SRAM aside from the storage array are realised by PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration) circuits. The storage uses 8T cell which will improve the browse margin and keep the write current against the synchronous read/write disturb.

All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The results indicated that the energy consumption of the adiabatic FinFET SRAM attenuated forty ninth compared with the SRAM supported CMOS devices [13].

From the above literature review it can be clearly observed that there exists a huge gap between the predicted power consumption of Memories (SRAMs) and real practical power consumption of SRAMs and there is a lot of scope of improving power consumption of SRAMs specially for low power portable devices. The adiabatic SRAM seems to be a promising solution for fulfilling efficient utilization of power in SRAMs.

III.   DESIGN OF PROPOSED ADIABATIC SRAM FOR PORTABLE DEVICES

The proposed adiabatic SRAM cell design is shown in Figure 1. The proposed adiabatic SRAM cell consists of four blocks: a read circuitry, a write circuitry, SRAM cell and address decoder. The MOS transistors M1 to M5 forms the read circuitry. The transistors M8 to M10 are used for address (column) decoder whereas the write circuitry is shown as combinational logic circuit synthesized using NOR gates and inverter. The Adiabatic SRAM is shown at center with bitlines (BL and BL') and wordlines (WL and WL'). The SRAM shown at center is driven by power clock. The adiabatic SRAM is based on the principle of charge recovery from the load capacitor back to the power clock to conserve the power.
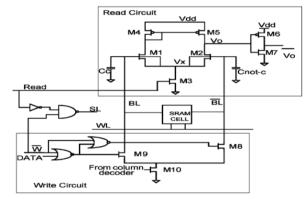

Figure 1: Proposed adiabatic SRAM cell design

IV.   DESIGN OF THE ADIABATIC SRAM

The adiabatic SRAM design is based on Dynamic Voltage Scaling (DVS) technique to reduce the leakage current and static power of the adiabatic SRAM cells and also retains the data stored during the idle mode. The leakage current reduces with operating voltage scaling in deep submicron processes because of short channel effects. The basic idea of the adiabatic SRAM is the use of two pass-transistors N4, N5 that provide different ground supply voltages to the adiabatic SRAM cell for normal and idle modes. The pass transistor N4 provide a positive voltage when the adiabatic SRAM cell is in idle mode and another pass transistor N5 provide a virtual ground when the cell is in active mode. The operating voltages of a memory cell are varied to switch between the active and idle (standby) modes that will give the less Leakage power significantly. The key idea of the adiabatic SRAM is the use of two pass-transistors that provide different ground supply voltages to the memory cell for normal and sleep modes. These pass- transistors provide a positive ground supply voltage when the cell is inactive and connect the cross-coupled inverters to the ground supply during normal operation to function as a conventional 6T-cell. The operating voltages of an array of memory cells are varied to switch between the active and stand-by modes and thus reducing the leakage power significantly. Both the access transistors (M5, M6) are high-Vt devices to further reduce the bit line leakage. Each of the pass gate used to control the source voltages of the NMOS transistors in the cross-coupled inverter is also a high-V, device to control the leakage current through these two pass transistors from the positive control voltage v to ground). None of the nodes is left floating when the cell is not in use and this ensures the stability of the stored

data with no additional complexity or circuitry. Since the capacitance of the ground supply lines is significantly less than that of the wells, this approach has improved transition time and energy as compared to others. Moreover, since the source voltage, as opposed to substrate voltage, is used to control the V, of the NMOS transistors during the sleep mode, the inherent problems associated with body bias are totally eliminated.

Reduction of the gate leakage current in the adiabatic SRAM cell can be done. The idea behind the adiabatic SRAM is to provide different ground levels of the memory cell in active and idle modes. During idle mode the positive voltage more than ground reduces the gate leakage and sub threshold currents of the adiabatic SRAM cell.
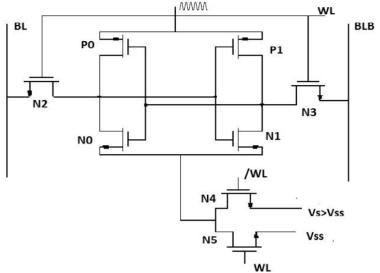

Figure 2: Basic Adiabatic SRAM cell

V.   RESULTS AND DISCUSSIONS

Adiabatic SRAM is implemented using OrCad PSPICE Simulator. The individual gate functionality and the overall logic is implemented using Structural style of Modeling .From the simulation results it is very much clear that the power dissipation of the proposed adiabatic SRAM is 25% lower than conventional 6T SRAM whereas the power dissipation is approximately 15% lower than 7T CMOS SRAM. Figure 3 shows the comparative analysis of the 6T conventional SRAM,
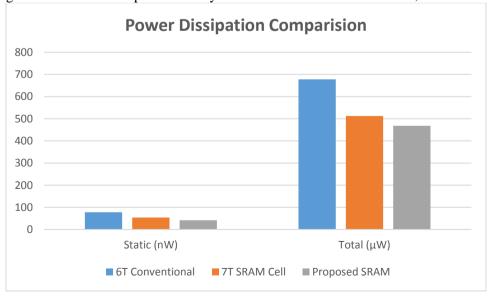

Figure 3: Power Comparison

Figure 4 shows the delay comparison analysis of the 6T conventional SRAM, 7T CMOS SRAM &

Proposed adiabatic SRAM. The proposed SRAM has a slightly higher propagation delay in comparison to 6T conventional & 7T CMOS SRAM cell.
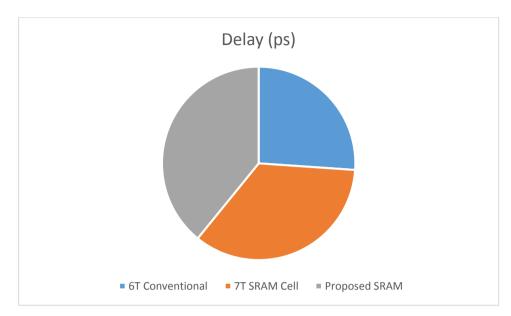

Figure 4: Delay comparison analysis

VI.   CONCLUSION

A novel approach for implementation of SRAM based on the principle of adiabatic is presented. The adiabatic SRAM can be implemented without significantly increasing size or complexity with an insignificant tradeoff of delay.so proposed adiabatic SRAM can be easily used for low power applications where latency is not a concern. Our design also provides the flexibility for possible optimizations of the SRAM from overall architectural considerations. Results indicate that the essential advantage of adiabatic logic that of low-power required for low power portable devices is achievable in presented adiabatic SRAM.

VII.   FUTURE WORK

This research contributes to better understanding of energy recovery techniques for SRAM. This work showed that the total energy and the energy during write cycle in particular will be saved in the designed Adiabatic SRAM.

1. The investigations reported in this work are for moderate memory size. However if bigger memories are to be realized, one has to look into memory organization problem from the point of writing, reading and hold mode.
2. Further new topologies for SRAM cells and bit line architectures should be explored to minimize the energy consumption.
3. The design approach can be done at abstract level. Analytical models for energy consumption in deep submicron technology SRAMs and those for performance parameters should be developed so that optimization of one can be done with respect to the other.

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AUTHORS BIOGRAPHY

Amit Saxena has 12 Years of experience in the field of Academic. He started his career from MIT, Moradabad. Presently he is working as an Assistant Professor, Deptt of E&C Engg., at MIT Moradabad. He obtained his Bachelor's degree in Electronics & Communication Engineering from I.E.T., Rohilkhand University, Bareilly and Masters degree (VLSI Design) in 2009 from UPTU, Lucknow. He is currently pursuing Ph.D. from Monad University, Hapur. He has published number of papers in international & national journals, conferences and seminars.

Kshitij Shinghal has 16 Years of experience in the field of Academic and is actively involved in research & development activities. He obtained his Doctorate degree from UPTU, Lucknow in 2013, Masters degree (Digital Communication) in 2006 from UPTU, Lucknow. He started his career from MIT, Moradabad. Presently he is working as an Associate Professor & Head, Deptt of E&C Engg., at MIT Moradabad. He has published number of papers in national journals, conferences and seminars. He has guided two Masters, more than sixty students of B. Tech, and guiding three Ph.D. & M. Tech. theses. He is an active Member of Various Professional Societies such as ISTE, IACSIT, IAENG etc.

Deepti Shinghal was born in Moradabad, Uttar Pradesh, India in January 1980. She received her Bachelor of Engineering (B.E.) degree in Electronics and Communication Engineering Rohilkhand University, Bareilly in 2000. Thereafter she worked for one year as a Faculty Member in the Department of Electronics and Communication Engineering at Aligarh Institute of Engineering & Technology, Aligarh. Then she joined the Moradabad Institute of Technology, Moradabad in 2002. She received her M. Tech. degree in VLSI Design from U. P. Technical University, Lucknow in the year 2008. She is pursuing Ph.D. from Monad University Hapur.