Adiabatic Power Clock for Reversible Logic

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ABSTRACT

Adiabatic logic circuits can offer significant reduction in power dissipation of logic circuits. However adiabatic logic circuits suffer from an inherent problem of increased number of components and latency due to increased switching times. Therefore, adiabatic logic circuits can be suitable for applications where switching is not the main concern. Another very important issue while designing adiabatic logic circuit is the realization of unconventional power supplies. Special type of power supplies (trapezoidal power clocks) are needed in adiabatic circuit configurations. This requirement of special type of power supplies results in an overhead both in terms of overall energy dissipation and silicon area. These issues should be carefully considered when adiabatic logic is used as a method for low-power design. This paper presents the power clock design for adiabatic logic circuit and functional simulation of the power clock.

KEYWORDS: *Adiabatic Circuits, Power Clock, Reversible Logic*

I. INTRODUCTION

Due to the typical features of CMOS technology, for integrating complex systems in small silicon area with fairly low power dissipation at speeds demanded by most of the applications, CMOS VLSI has been the obvious choice of designers. About 90% of the total electronic systems use CMOS technology at the back end. CMOS technology has as edge over other device technologies as far as power dissipation is concerned. The three contributory factors to the total power dissipation in CMOS are : a) Static Power Dissipation under steady state due to reverse leakage current of p-n junctions and subthreshold leakage current (≈ 15% contribution to total power dissipation) , b) Dynamic Power Dissipation due to charging and discharging of load capacitance during switching (≈ 70-75% contribution to total power dissipation) and c) Short Circuit Power Dissipation due to direct low resistance path between supply and ground again during switching. (≈ 10% contribution to total power dissipation). Hence number of solutions at architectural level and circuit level have been proposed in the literature to primarily reduce dynamic power dissipation and then leakage & short circuit power dissipation of CMOS circuits. Though, over a period of time an appreciable reduction in power dissipation and hence energy consumption has been achieved, one of the draw- backs of CMOS circuits are that energy is continuously drained out from the power supply. Adiabatic logic technology has been proposed as one of the ways to conserve and recover energy thereby offering energy efficient solutions to electronic systems. A key aspect in the evaluation of the potential and the perspectives of adiabatic logic families is the design and simulation of the power clock generator. Most of the adiabatic logic families require a two-phase or a four-phase clock. Adiabatic power clock generator requires additional circuit (off the chip or on the chip) which increases the circuit complexity with respect to standard CMOS solutions.in general power clock has two phases consisting of rise time and fall time. During the rise time the clock charges the node capacitances to the voltage required for the operation of the logic circuit, and during the fall time it recovers the energy just stored in the node capacitances. If the rise and fall times of the power clock are much larger than the time constants associated to the capacitances of the circuit, such energy transfers occur almost ‘adiabatically’, i.e. without energy loss. With this aim, in this paper we propose a high efficiency four-phase trapezoidal power supply generator

for adiabatic logic circuits. The main specifications for a DC/AC converter for adiabatic circuits are the capability to recover the energy stored in the load capacitances, and a high power-conversion efficiency defined as the ratio of the load power to the total DC supply power. Oscillators based on LC resonant circuits can meet these requirements and therefore ensure that the complete adiabatic system provides significant power savings with respect to its standard CMOS counterpart.
Rest of the paper is organized as follows. Section 1 covers brief introduction of adiabatic principles with types of adiabatic logic. Section 2 covers the design methodology followed by section3 which covers the simulation setup and results discussion followed by conclusion.

II. ADIABATIC PRINCIPLE

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design.

- **Never turn *on* a transistor if there is a voltage across it (V_{DS}>0)**
  1. The inputs must be valid during the charging/discharging process
  2. Make sure every node is reset to the original stage before performing the next operation**.**
- **Never turn *off* a transistor if there is a current through it ($I_{DS}\neq 0$)**
  1. The inputs must be held static throughout the charging and discharging of capacitances
  2. Ensure high resistance results in more energy consumption
- **Never pass current through a diode**

If these conditions with regard to the inputs, in all the four phases of power clock, recovery phase will restore the energy to the power clock, resulting considerable energy saving. Yet some complexities in adiabatic logic design perpetuate. Two such complexities, for instance are:

- Circuit implementation for time-varying power sources (power clock) needs to be done.
- Computational implementation by low overhead circuit structures needs to be followed.

III. POWER SUPPLIES FOR ADIABATIC CIRCUITS

The design of a power clock is an important part of the whole adiabatic system design. Many studies on adiabatic logic design have been made and various approaches have been proposed. All of them require extra circuitry for one or more time- varying power sources to provide extended charging time. There are methods such as those using either inductive power supplies. This is often done using inductors, which store the energy by converting it to magnetic flux. This has been used because many adiabatic circuits use a combined power supply and clock, or a “power-clock”. This a variable, usually multi-phase, power-supply which controls the operation of the logic by supplying energy to it, and subsequently recovering energy from it. Because high-Q inductors are not available in CMOS, inductors must be off-chip, so adiabatic switching with inductors are limited to designs which use only a few inductors. Quasi-adiabatic stepwise charging avoids inductors entirely by storing recovered energy in capacitors. Stepwise charging (SWC) can use on-chip capacitors, step-wise charging through banks of capacitance tanks, or resonant drivers, etc.

3.1 Phases in an Adiabatic Power Supply

The constant-current source needed for the adiabatic operation is usually a trapezoidal or, sinusoidal voltage source. In an adiabatic circuit, the power supply also acts as a clock. Hence,

it is given the term "power clock". A single-phase sinusoidal power-clock can easily be generated using resonant circuits.

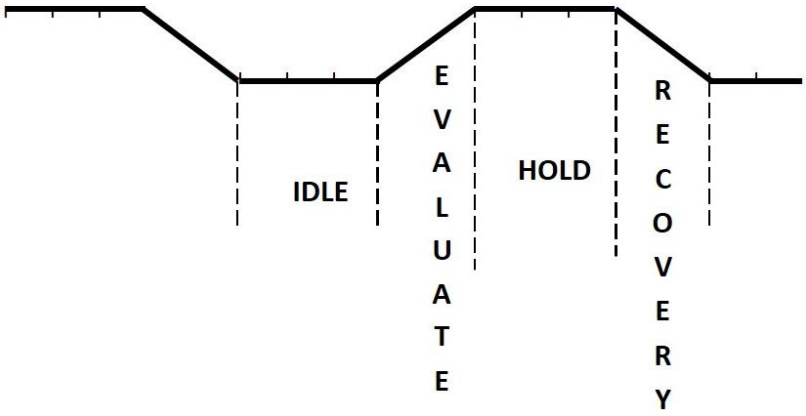

Figure1: A trapezoidal adiabatic power supply showing different phases.

Initially, the adiabatic supply is in the IDLE / WAIT phase and the supply voltage is LOW maintaining at the same time the outputs in the LOW state. Then the inputs are set (one goes LOW the other HIGH) and the supply voltage ramps-up. As the inputs are evaluated, the outputs change complementary to each other and the one that goes HIGH follows the power supply until it reaches VDD. At that moment the inputs are returned to the LOW state and after a certain period of time in the HOLD "1" phase, the supply ramps down with the outputs following until the LOW state is reached again. That is, to say, during the IDLE/ WAIT phase, the circuit idles. In the EVALUATE phase, the load capacitance either charges up or does not, depending upon the inputs to the functional blocks. In the HOLD phase, the output is kept at steady, so that the subsequent stage can evaluate. Finally, in the RECOVERY/ RESET phase, the charge held on the capacitance is recovered. Any digital system with multiple stages/ cascades based upon the described adiabatic power clocking scheme must have at least four clocks, each leading its previous phase by 90°. Practical adiabatic circuits use sinusoidal power clock. This is an approximation of the trapezoidal waveform with the duration of the hold phase tending to zero.

IV. DESIGN OF AN ADIABATIC POWER SUPPLY

There are several ways to implement a clock generator:
One way is to use an external inductance as shown in Figure 2. The resulting circuit is a resonant LC circuit with the major difficulty that the C of the LC is the switched capacitance of the circuit so dependent on the specific design of the circuit. The adiabatic power supply needs an efficient energy recovery design which implies quality factor Q of the power supply to be very high. Not only the Q should be high, it should be proportional to the cycle time so that the energy dissipation in the power supply should also decrease with the frequency. Otherwise, dissipation in the power supply itself will dominate the logic circuit dissipation at lower frequencies. Most preferable technique is to use sinusoidal voltage supply because of its ease to design as compared to the pure trapezoidal wave. The constant current charging needed can be approximated using a sinusoidal power supply. Thus, an LC resonant circuit is created and the energy is oscillated between the external inductor and the capacitances to be switched. In inductor based approach energy can be circulated between electrostatic field in the load capacitor and magnetic field in the off-chip inductor. Analysis of this approach shows that by applying sinusoidal ramp, energy saved in the circuit is reduced significantly as compared to pure trapezoidal wave.

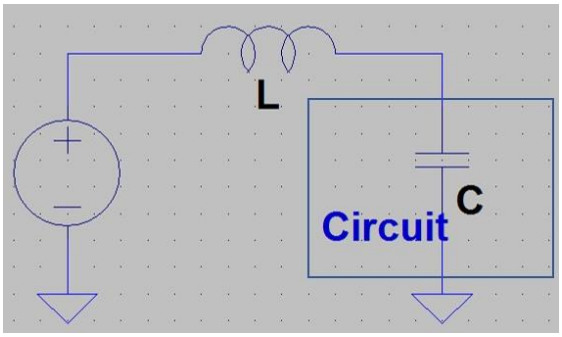

Figure 2: Resonant LC circuit for Power Clock Generation

To use a simple circuit as shown in Figure 2 based on capacitors in which charges are saved when the load capacitor is discharged. The basic idea is to have several supply voltages realized with big capacitors and associated switches. The switches with each capacitor are controlled by a logic to provide supply through the charges to the output when it is switching 'on' and to save charges when the output switches 'off'. Furthermore, switches are working at Vdd/4 and not at Vdd.

The output capacitance is charged to Vdd/4 through the first switch, then to Vdd/2 with the second switch and so on to reach Vdd. This charge is slow, as each charge has a duration of 3*RC. The discharge is performed through the second switch from the top, then the third switch connected to Vdd/2 and so on. The last charge from Vdd/4 to Vss is lost.

For each step, 0.5 *C*(Vdd/4)2 = C*Vdd2/32 is dissipated in the switch and charge C*Vdd/4 is stored in the CL capacitance. For the 4 steps, 4 * C*Vdd2/32 is dissipated in the switches, i.e. C*Vdd2/8, which is 4 times less compared to a conventional inverter. With N Vdd levels, it would be N times less (ideal case).

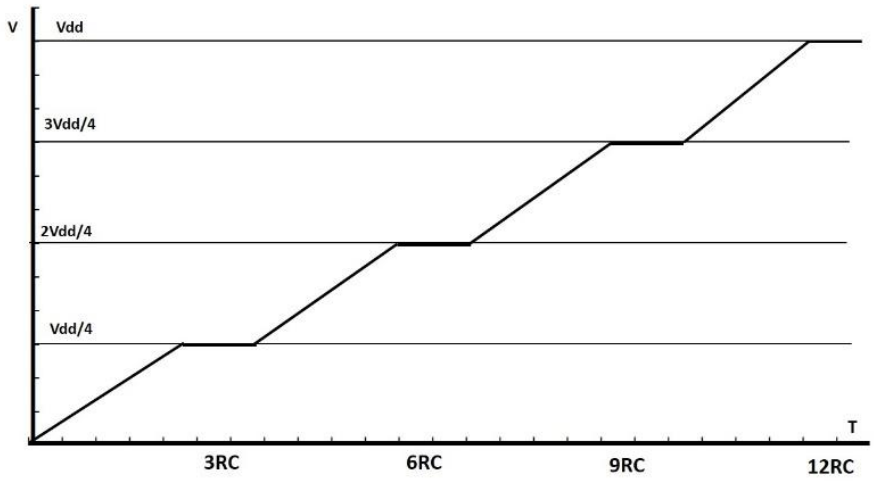

Figure 3: Stepwise charge-up

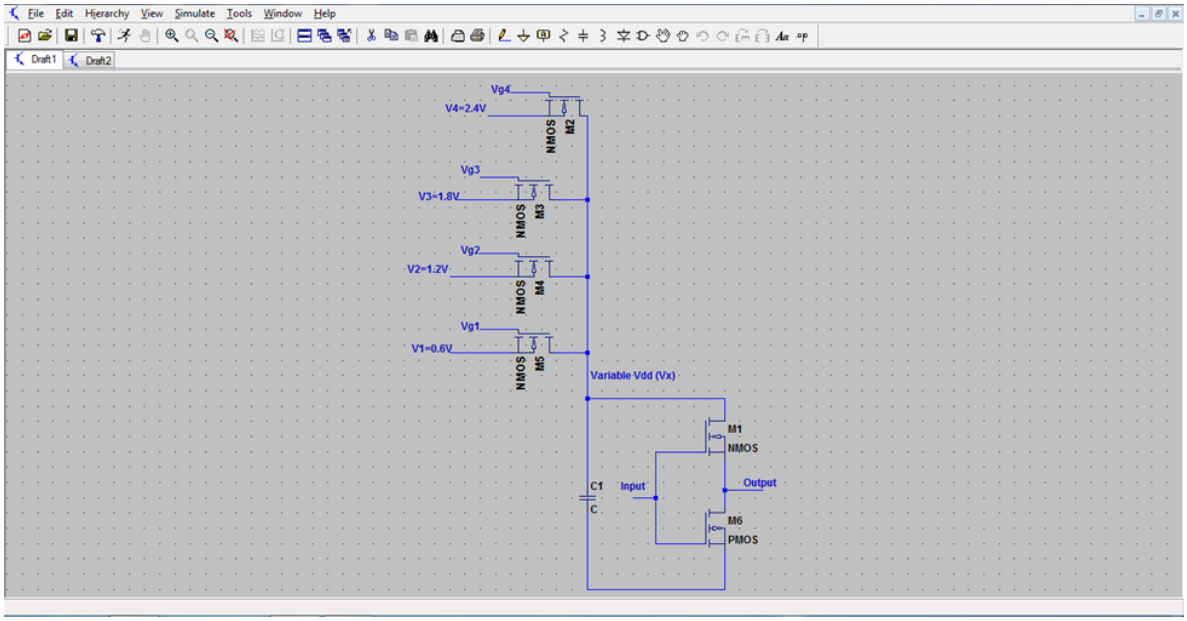

Figure 4: Stepwise driver circuit for capacitive loads.

Adiabatic Logic with power supplies with slow ramps

The energy required to do an adiabatic switching depends on the working frequency where Tclk is the working period. Increasing Tclk results in decreasing the energy necessary to any computation. Such a technique is based on two principles:

- Switching the nodes in a smooth way, i.e. with no voltage between drains and sources of transistors
- Recovering the charges stored in the circuit for later reuse.

where RC is the delay of the considered gate. Therefore, if T is larger than RC, energy can be saved and if T is infinite, no energy is used.

Special power supplies must be used: they have to oscillate to perform the smooth switching and they have to recover the charges that the circuit stores without dissipating energy.

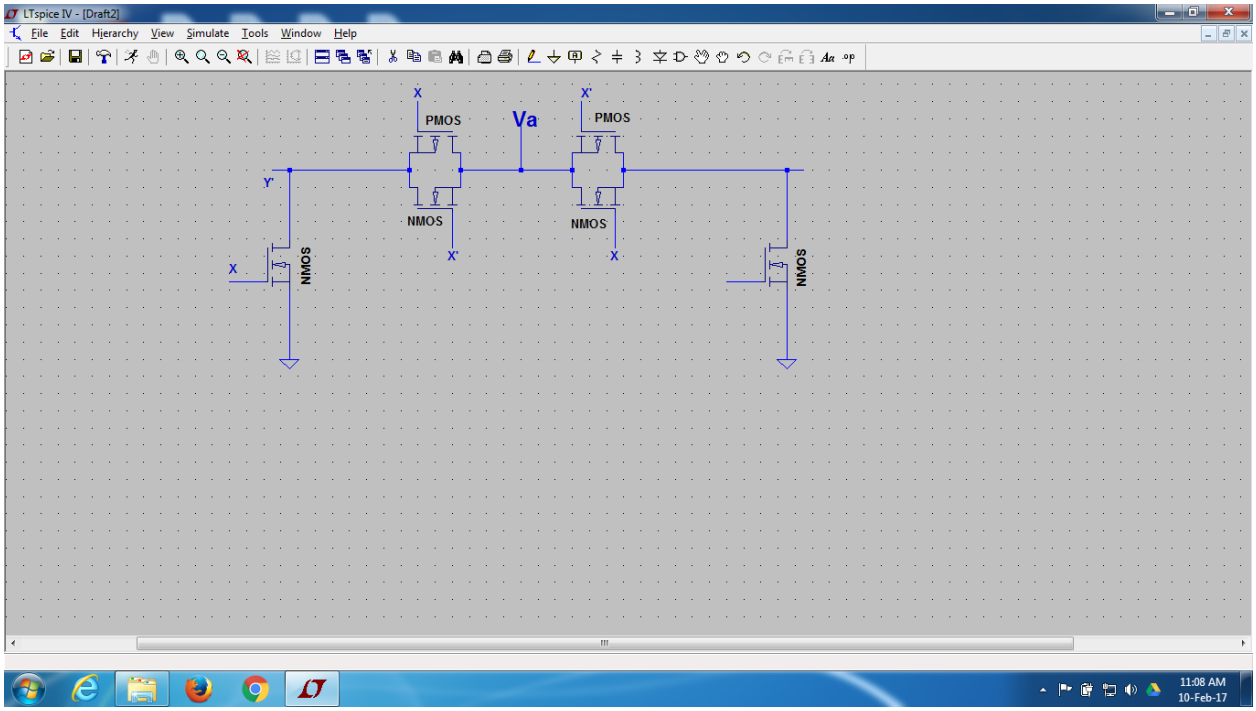

Figure 5: Adiabatic amplifier circuit which transfers the complementary input signals to its complementary outputs.

The basic idea is to determine the input state (for instance IN=0 for an inverter) and then to have a slow ramp 0->1 for the power supply, as shown in Figure 4. As long as the power supply is at "1", the output S presents the right output value. It has to be used or stored when the power supply is on. Now, with the inputs always active (IN=0), the power supply has to switch off smoothly 1->0. In such an 2 adiabatic discharge, the ½ C Vdd stored in the output capacitance has to be recovered by the power supply. All the charges go through the P-ch transistor back to the power supply (and not to the ground) without any dissipation in the P-ch transistor. Such a mechanism is called "logic reversibility".

V. CONCLUSION AND FUTURE WORK

Our study showed that adiabatic logic circuits provide a method of decreasing the energy dissipation when compared with conventional logic switching under certain circumstances. With adiabatic circuits, all input signals must undergo a controlled transition in the form of a ramp, unlike the conventional logic switching where only the input signals which have different final logic state change. This overcomes the inherent crowbar dissipation associated with slow logic signal transitions. However adiabatic logic circuits require a special type of power supply for their operation. The power clock for adiabatic logic circuit was designed and simulated. Results confirmed to the proposed solution for the adiabatic power supply. The use of transmission gate logic elements provides an elegant solution to producing logically and physically reversible functions. Unlike other forms of reversible logic, a separate physical reverse logic path is not required as these gates can operate in both directions, they are physically and logically reversible. However the overriding contribution to energy dissipation is that generated by switching losses and this class of circuit operated in this manner does not at present offer a realistic solution to low energy reversible computing.

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