A Survey Paper on Reversible Arithmetic and Logical Unit

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ABSTRACT

In VLSI, CMOS technology is dominant due to its lots of advantages. In MOS technology, the voltage is applied to insulated gate controls current between source and drain. It is called low power technology. Low power allows very high integration. The complexity of integrated circuits increases day by day. Hence power dissipation has become the main area of concern in VLSI design. In earlier, various techniques were used to reduce power dissipation. Now a day's Reversible logic can be used as an alternative. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. It has wide applications in low power CMOS and optical information processing, Digital signal processing, Computer graphics and Cryptography. In this paper, a new method is proposed for designing reversible logical unit. A decoder unit is used for controlling the operations of logical unit. All the modules are being designed using the basic reversible gates.

KEYWORDS: *Reversible logic, Reversible gates, Constant input, Garbage output*

I. INTRODUCTION

In modern VLSI system million, billions of transistors are incorporated on same chip. For implementation, CMOS technology is dominant. This technology has lots of advantages over bipolar junction technology. The two important characteristics of this technology are high noise immunity and low static power consumption. The complexity of VLSI circuits increases day by day, along with power consumption power dissipation is also main concerned for designing of integrated circuits. According to Moore's law, the number of transistors on integrated circuits doubles approximately every two years. Hence power dissipation by these also increases. In Conventional logic circuits, every time one bit information is lost during computation hence heat is generated due to the loss of bit. In order to avoid this loss of information the Conventional circuits are designed using Reversible logic. Landauer [1961], shows that for conventional logic computations, each bit of information lost, generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1].Bennett showed that kTlog2 energy dissipation would not occur, if a computation is carried out in a reversible way [2].i.e. no amount of energy would be dissipated from a system as long as the system was able to return to its initial state from its final state regardless of what occurred in between. This paper is organized as follows: Section 2 gives Literature review. Section 3 gives the brief introduction about the reversible logic gates and ALU. Section 4 describes the proposed methodology for reversible ALU.

II. LITERATURE REVIEW

Landauer, Rolf. [1]." Irreversibility and Heat Generation in the Computing Process". R Landauer's showed, amount of heat generation due to loss of bit is kTlog2, and this value is approx $2.8*10^{-21}$ joule, which is small but not negligible. Bennett, Charles H [2]. "Logical Reversibility of Computation". Bennett showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates. No amount of heat would be dissipated from the system as long as the system was able to return to its initial state from its final state. E.Fredkin, T Toffoli, Peres [3] [4] [5] proposed reversible logic gates. In "An Arithmetic Logic Unit Design Based on Reversible Logic Gates" [8] Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang, Lihui Ni. Proposed a method for using the reversible logic gates as logic devices to structure the reversible

ALU. In "Design and Analysis of 16 bit reversible ALU". Lekshmi Viswanath, Ponni.M [7], presented that circuit designed using reversible logic has reduce delay and power.

III. RELATED WORK AND PROBLEM DESCRIPTION

A reversible gate is simply one that computes a bijective function. This means that there are exactly as many output bits as input bits. Reversible logic is gaining importance in area of CMOS design because of its low power dissipation. The two main limitations of reversible logics are feedback or loops are not allowed and fan out s are not allowed. A gate is considered to be reversible only if for each and every input there is a unique output assignment, and this can be achieved with the help of constant inputs (CI) and garbage outputs (GO).The main criteria of reversible logic are minimized the number of constant inputs and garbage outputs.

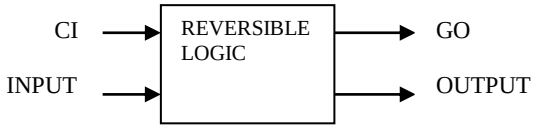

Figure 1 Block Diagram Representation.

Basic Reversible Logic Gates:

A gate with k inputs and k outputs is called a k × k gate or a gate on k wires. The number of reversible (3, 3) gates is 8! Which is equals to 40320 combinations. But not every pair of balanced function of 3 variables may appear in a reversible (3, 3) gate.

2.1. Feynman gate

It is a 2*2 gate, having 2 inputs and 2 outputs. The input vector is I (A, B) and the output vector is O (P, Q). Shown in figure 2.

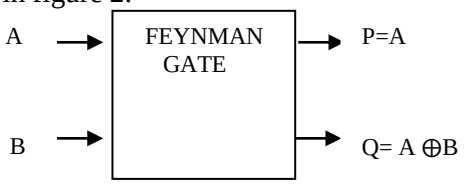

Figure 2 Feynman Gate

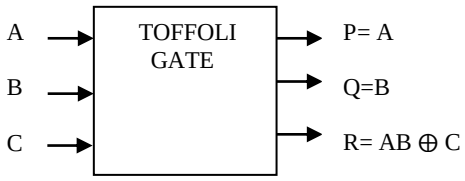

Figure 3 Toffoli Gate

2.2. Toffoli gate [4]

It is a 3*3 gate, having 3 inputs and 3 outputs. The input vector is I (A, B, C) and output vector is O (P, Q, R).shown in figure 3.

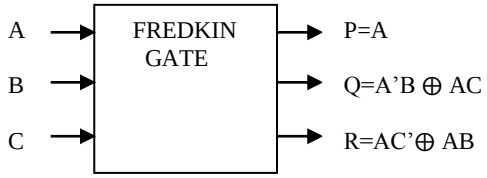

Figure 4 Fredkin Gate

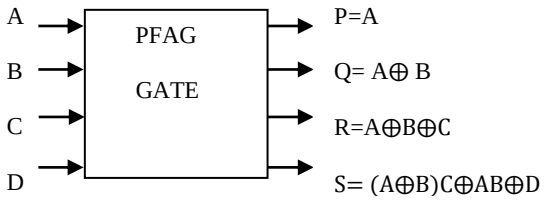

Figure 5 PFAG Gate

2.3. Fredkin gate [3]

It is a 3*3 gate, having 3 input and 3 output .The input vector is I (A, B, C) and output vector is O (P, Q, R). Shown in figure 4.

The 4x4 combinations are also possible. The 4x4 reversible gates include TSG gate, MKG gate, HNG gate, PFAG gate shown in figure 5 etc. Some of the 4x4 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above mentioned gates can be used in the design of reversible adders.

IV. ARITHMETIC AND LOGICAL UNIT

ALU performs arithmetic function such as addition, subtraction, multiplication and logical function such as AND, OR, NOT, NAND, XOR operation. In computing, an arithmetic and logic unit (ALU) is a circuit that performs integer arithmetic and logical operations. It is a fundamental building block of the central processing unit of a computer. So it must be fast and should dissipate less power.

V. PROPOSED METHOD

Till now, different ways have been found to design arithmetic and logical unit. Methods have been designed to reduce the power dissipation and reduce the delay of unit. In this paper, a new method is proposed that make existing logical unit reconfigurable. A decoder circuit can be designed instead of designing of each module. Thus this circuit contains adder/sub module, multiplier module and a logical module which performs its operation according to the input of decoder. The proposed methods have been summarized by the block diagram.

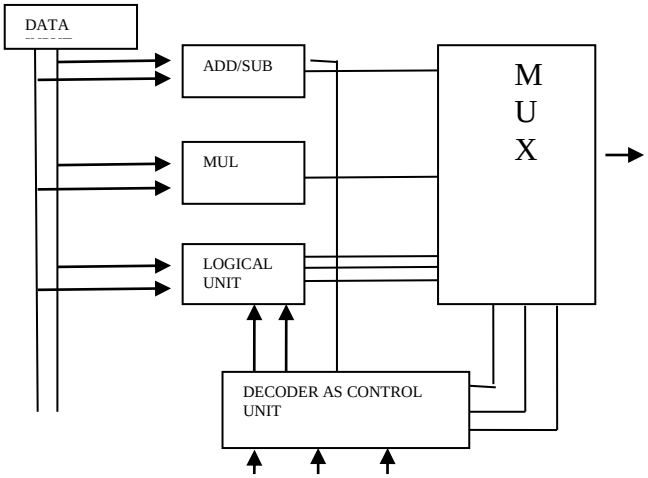

Figure 5 Block Diagram of proposed method

VI. CONCLUSIONS

Instead of designing every module of logical unit, a reconfigurable unit can be designed. This reconfigurable unit can be achieved by decoder circuit which acts as control unit. This control unit will take decision that which operation should be performed. Hence gate count will reduce and power dissipation also.

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REFERENCES

[1] Landauer, Rolf." Irreversibility and heat generation in the computing process. "IBM journal of research and development 5.3 (1961): 183-191.

[2] Bennett, Charles H. "Logical reversibility of computation." IBM journal of Research and Development 17.6 (1973): 525-532.

[3] E Fredkin, T Toffoli, "Conservative Logic", International Journal of Theory. Physics,21 (1982),pp 219-253.

[4] T. Toffoli. "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science.

[5] A. Peres, *"Reversible* Logic and Quantum computers", Physical review A, 32: 3266-3276, 1985.

[6] N.Srinivasa Rao, P.Satyanarayana "A Novel Reversible Gate and its Applications*"*. IJET Volume 2 No.7, July, 2012.

[7] LekshmiViswanath,Ponni.M' 'Design and analysis of 16 bit reversible ALU", IOSR Journal of Computer Engineering (IOSRJCE) ISSN : 2278-0661 Volume 1, Issue 1 (May-June 2012), PP 46-53

[8] Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang, Lihui Ni "An Arithmetic Logic Unit design based on reversible logic gates"IEEE Pacific Rim Conference on Communications, Computers and

Signal Processing (PacRim), 2011

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