

A Novel Designing Approach for Low Power Carry Select Adder

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ABSTRACT

Carry select adder (CSLA) is known to be the fastest adder among the conventional adder structures. Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using D latch. Experimental results are compared and the result analysis shows that the proposed architecture can drastically reduce the area and power.

KEYWORDS: Area efficient, CSLA, BEC, D-Latch

I. INTRODUCTION

Area and power have major role in the designing of integrated circuit because of the increase in popularity of portable systems as well as the rapid growth of power density in VLSI circuits. Addition usually influences strongly on the overall performance of digital systems and a crucial arithmetic function. Adders are most widely used in electronic applications. For example, in microprocessors, millions of instructions per second are performed. Due to the increase in the portability of the devices like mobile, laptop etc. require more battery backup. Low power and area efficient addition and multiplication have always been a fundamental requirement of high performance processors and systems. Designing efficient adder is the most difficult problem for researchers in VLSI design. The carry-select adder (CSLA) provides a compromise between small area but longer delay ripple carry adder (RCA) and larger area with shorter delay carry look-ahead adder [6]. CSLA uses multiple pairs of ripple carry adder (RCA) to generate partial sum and carry by considering carry input $C_{in}=0$ and $C_{in}=1$, then the final sum and carry are selected by multiplexers (mux) [3]. The modified CSLA using BEC [2, 4, 6] has reduced area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by reducing the group. The proposed architecture reduces the area and power.

II. AREA AND DELAY CALCULATION

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. Then add up the number of gates in the longest path of a logic block that contributes to the maximum delay.

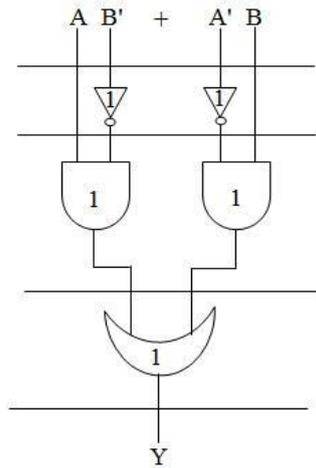


Figure 1. Delay and Area Evaluation of an XOR Gate

The area evaluation is done by counting the total number of AOI gates required for each logic block. The delay calculation is done by using the parallel performance of work in XOR gate. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and Full Adder (FA) are evaluated and listed in Table 1.

Table 1 Delay and Area count of the blocks of CSLA

Adder Blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

III. REGULAR CARRY SELECT ADDER

A 16-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size. Similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least-significant bit to the most-significant bit. The various 16, 32, 64 and 128-bit CSLA can also be developed by using ripple carry adders. The speed of a carry-select adder can be improved up to 40% to 90%, by performing the additions in parallel, and reducing the maximum carry delay. Figure 2 shows the regular structure of 16-bit SQR CSLA.

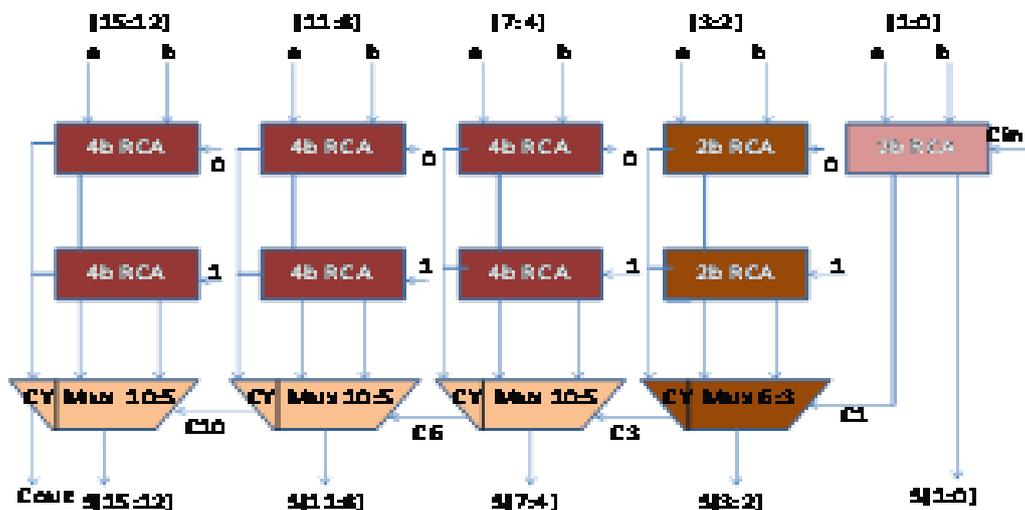


Figure 2. Regular SQR carry select adder

It includes many ripple carry adders of variable sizes which are divided into groups. Group 0 contains 2-bit RCA which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [1:0] and the carry out. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the corresponding RCA (Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups. In Regular CSLA, there is only one RCA to perform the addition of the least significant bits [1:0]. The remaining bits (other than LSBs), the addition is performed by using two RCAs corresponding to the one assuming a carry-in of 0, the other a carry-in of 1 within a group. In a group, there are two RCAs that receives the same data inputs but different Cin. The upper adder has a carry-in of 0, the lower adder a carry-in of 1. The actual Cin from the preceding sector selects one of the two RCAs. That is, as shown in the Fig.2, if the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected. For this Regular CSLA architecture, the implementation code, for the Full Adders and Multiplexers of different sizes (6:3, 8:4, 10:5) are designed. The delay and area count of a regular carry select adder is shown in the table 2.

Table 2 Delay and area count of regular SQR CSLA groups

Group	Delay	Area
Group2	11	57
Group 3	13	87
Group4	16	117
Group5	19	147

IV. MODIFIED CARRY SELECT ADDER

The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The modified 16-bit CSLA using BEC is shown in Figure 3. The structure is again divided into five groups with different bit size RCA and BEC.

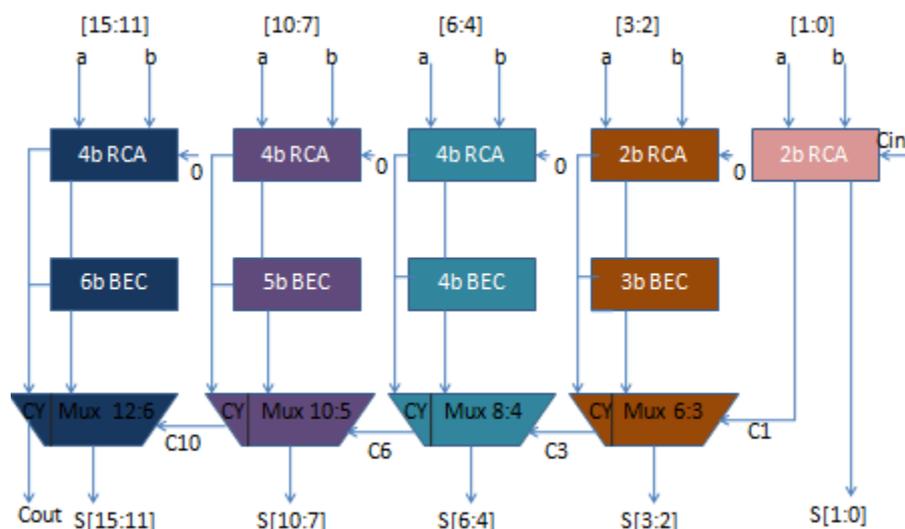


Figure 3. Modified Carry Select Adder

One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA [8]. By manually counting the number of gates used for group 2 is 43 (full adder, half adder, multiplexer,

BEC). The delay and area count of modified SQRT CSLA is listed in table 3.

Table 3. Delay and Area Count of modified SQRT CSLA

Group	Delay	Area
2	13	43
3	16	61
4	19	84
5	22	107

V. PROPOSED CARRY SELECT ADDER

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their input. Figure 4 shows the proposed carry select adder.

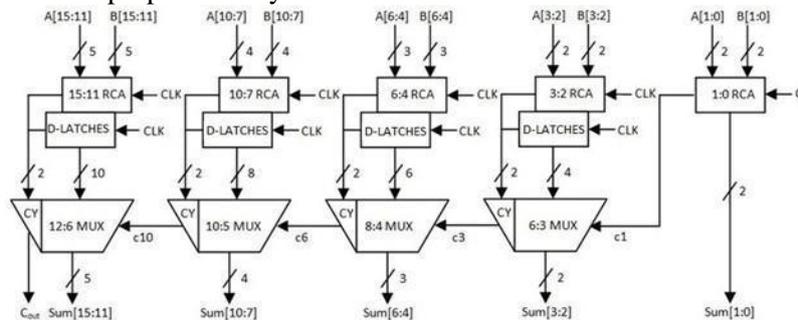


Figure 4 .Proposed Carry Select Adder

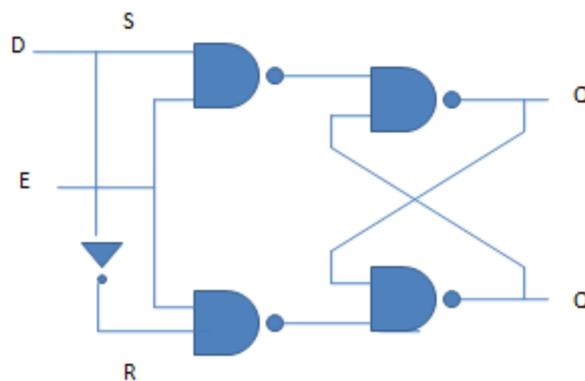


Figure 5.D Latch

This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. it can understand that latch is used to store the sum and carry for $C_{in}=1$. Carry out from the previous stage i.e, least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. C_{out} is the output carry. The internal structure of group 2 of the proposed 16-bit CSLA. The group 2 performed the two bit addition which are a_2 with b_2 and a_3 with b_3 . This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2.

The group 2 structure has three D-Latches in which two are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer

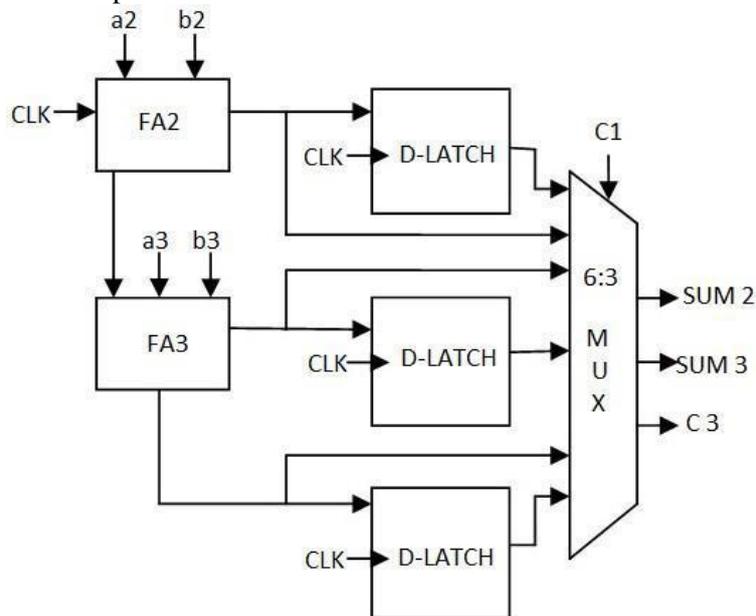


Fig.6 .Group 2 Structure

When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the D-Latch is not enabled. When the clock is high, the addition is performed with carry is equal to one. All the D-Latches are enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

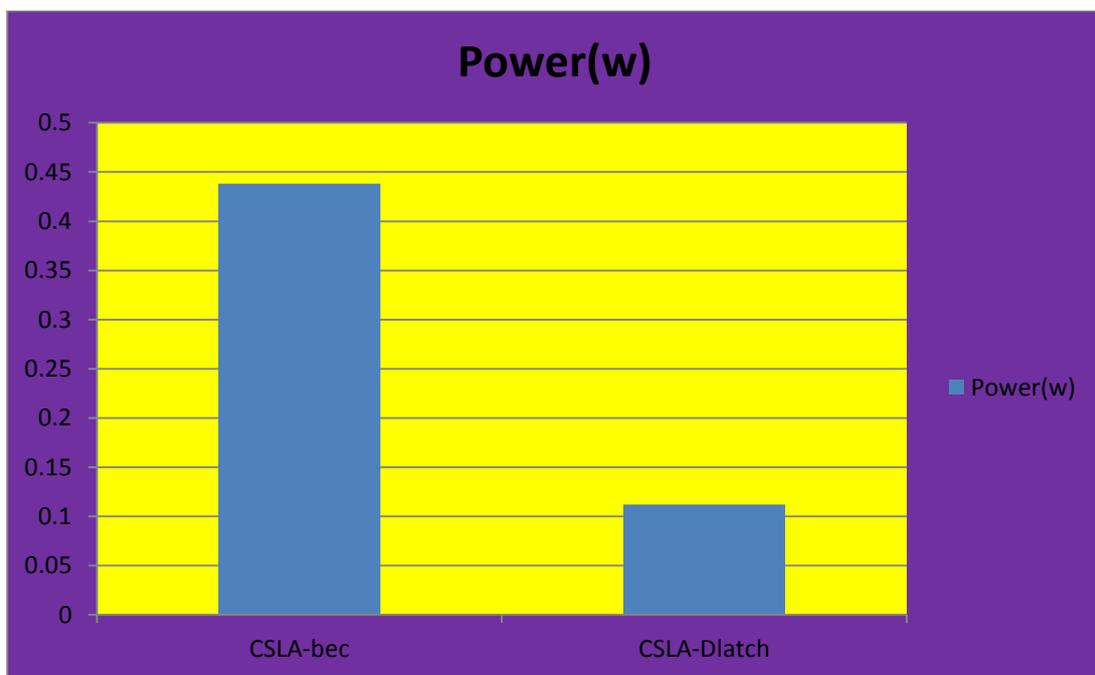
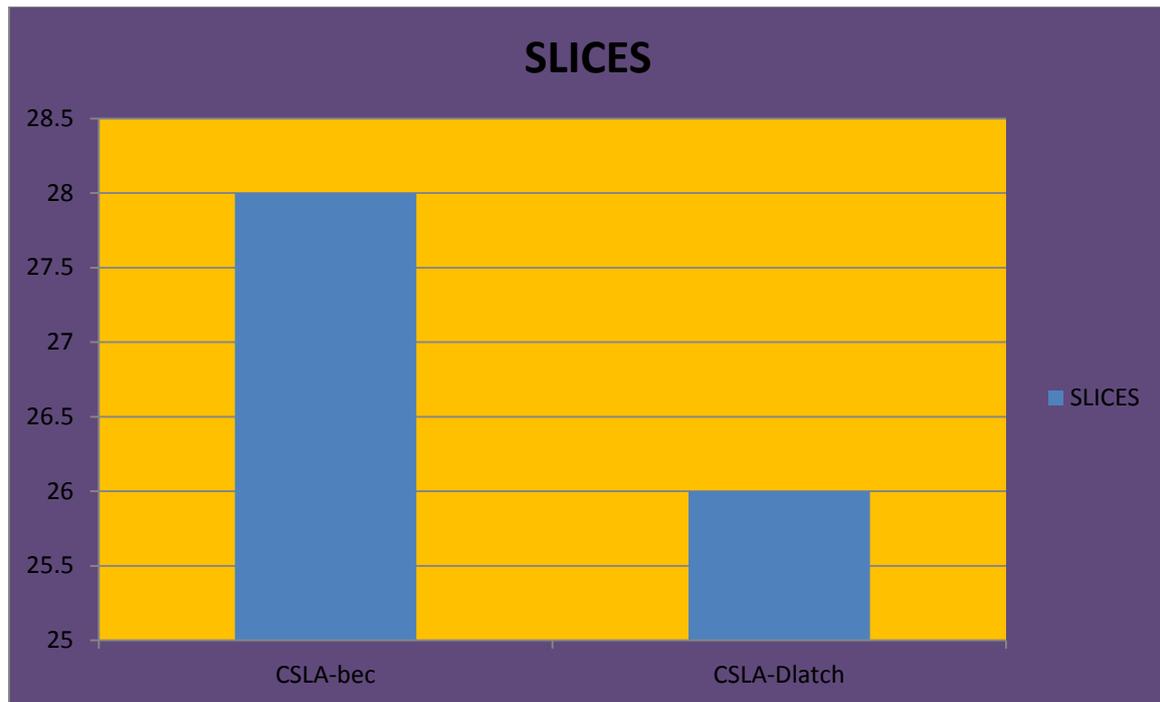
VI. COMPARISON RESULT

We perform the simulation and synthesis and summarize the results of modified CSLA and CSLA using D-Latch. The functional verification and synthesis of all the adders are performed and results are summarized.

Table 4. Comparison of CSLA parameters

ADDER	Area(No of slices)	Power
Modified CSLA	28	0.412
Improved CSLA	26	0.112

experimental results



VII. CONCLUSION

A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. Regular CSLA suffers from the disadvantage of occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the area and power than regular and modified CSLA by the use of D-latches.

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